Product Specifications

Customer	
Description	**7.4” TFT EPD Panel**
Model Name	**EW074CT011**
Date	**2016/04/22**
Doc. No.	**1P109-00**
Revision	**03**

Customer Approval	
Date	
The above signature represents that the product specifications, testing regulation, and warranty in the specifications are accepted	

	Design Engineering		
	Approval	**Check**	**Design**
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Revision History

Version	Date	Page (New)	Section	Description
01	2015/08/24	All	All	Specification first issued
02	2016/03/11	27	7	Update Figure 7 1 Packing Diagram
		33	9	Update Figure 9 3 Carton Label
03	2016/04/22	12	2.1	Modify Note (2)

Glossary of Acronyms

EPD	Electrophoretic Display (e-Paper Display)
EPD Panel	EPD
EPD Module	EPD with TCon board
TCon	Timing Controller
TFT	Thin Film Transistor
FPC	Flexible Printed Circuit
FPL	Front Plane Laminate
SPI	Serial Peripheral Interface
COG	Chip on Glass
PDI	Pervasive Displays Incorporated

1 General Description

1.1 Overview

This is a 7.4" a-Si TFT active matrix Electronic Paper Display (EPD) module. The module has such high resolution (126 dpi) that it is able to easily display fine patterns. Due to its bi-stable nature, the EPD module requires very little power to update and needs no power to maintain an image.

1.2 Features

- a-Si TFT active matrix Electronic Paper Display(EPD)
- Resolution: 480 x 800
- Ultra low power consumption
- Super Wide Viewing Angle - near 180°
- Extra thin & light
- SPI interface
- RoHS compliant
- Wide temperature support

1.3 Applications

- e-POP/Signage
- Electronic bulletins
- Office Automation
- Navigator

1.4 General Specifications

Table 1-1 General Specification

Item	Specification	Unit	Note
Outline Dimension	111.0(H) x 169.0(V) x 1.2(T)	mm	(1)
Active Area	96.96(H)x 161.6 (V)	mm	
Driver Element	a-Si TFT active matrix	-	
FPL	Aurora Mb	-	
Pixel Number	480 x 800	pixel	
Pixel Pitch	0.202 x 0.202 (126dpi)	mm	
Pixel Arrangement	Vertical stripe	-	
Display Colors	Black/White	-	
Surface Treatment	Anti-Glare	-	

Note (1): Not including the FPC.

1.5 Mechanical Specifications

Table 1-2 EPD Mechanical Specification

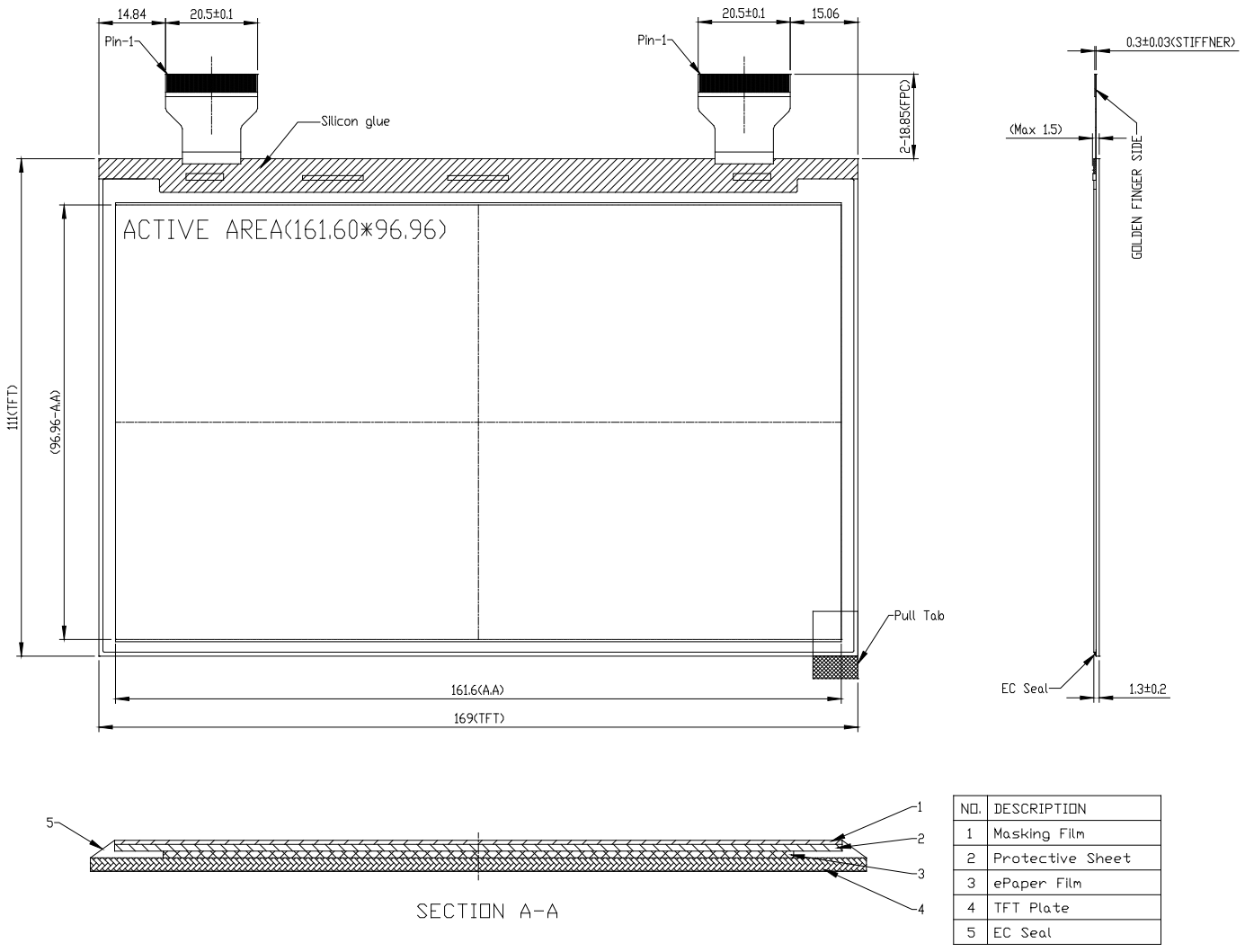
Item		Min.	Typ.	Max.	Unit	Note
Glass Size	Horizontal(H)	168.7	169.0	169.3	mm	
	Vertical(V)	110.7	111.0	111.3	mm	
	Thickness(T)	1.0	1.2	1.4	mm	(1)
Weight			43.9	52.7	g	

Note (1): Not including the Masking Film.

Table 1-3 FPC Specification

Item	Pin numbers	Pitch (mm)	Connector	Note
Golden Finger	40	0.5	STARCONN 089H40 or HRS TF31-40Sor Compatible	

Figure 1-1 EPD Drawing



NO.	DESCRIPTION
1	Masking Film
2	Protective Sheet
3	ePaper Film
4	TFT Plate
5	EC Seal

General tolerance: ±0.3mm

2 Absolute Maximum Ratings

2.1 Absolute Ratings of Environment

Table 2-1 Absolute Ratings of Environment

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature (*)	T_{ST}	-20	+60	ºC	(1), (3)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2), (3)

Note (1):

(a) 90 %RH Max. (Ta ≦ 40 ºC), where Ta is ambient temperature.

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation and no frost.

(d) If users like to put the EPD under some extreme condition (e.g. +60 ºC, < 30% RH), the lifetime of EPD may be shorter than warranty lifetime. Please contact PDi sales respective for details.

Note (2): The temperature of panel display surface area should be 0 ºC Min. and 50 ºC Max. Refresh time depends on operating temperature.

Note (3): In order to keep good performance of EPD, please refer to precaution for storage condition.

2.2 Reliability Test Item

Table 2-2 Reliability Test Items

Item	Test Condition	Remark
High Temperature Operation	50 ℃ / 30 %RH for 240h	(1) (2)
Low Temperature Operation	0 ℃ for 240h	(1) (2)
High Temperature/Humidity Operation	40 ℃ / 90 %RH for 168h	(1) (2)
High Temperature Storage	60 ℃ / 30 %RH for 240h	(1)(2)(3)
Low Temperature Storage	-20 ℃ for 240h	(1)(2)(3)
High Temperature/Humidity Storage	50 ℃ / 80 %RH for 168h	(1)(2)(3)
Thermal Cycles (Non-operation)	1 Cycle:-20℃/30min → 60℃/30min, for 100 Cycles	(1)(2)(3)
Package Drop Test	Drop from 97cm. (ISTA) 1 corner, 3 edges, 6 sides. One drop for each.	(1)(2)(3)
Package Random Vibration Test	1.15Grms, 1Hz ~ 200Hz. (ISTA)	(1)(2)(3)

Note (1): No condensation and no frost during test. End of test, function, mechanical, and optical shall be satisfied.

Note (2): The test result and judgment are based on PDI's 1bit driving waveform, driving fixture and driving system.

Note (3): Stay white pattern for storage and non-operation test.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings of Panel

Table 3-1 Absolute Maximum Ratings of Panel

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{DD}	-0.3 to +7	V
Source positive supply voltage	V_{POS}	-0.3 to +20	V
Source negative supply voltage	V_{NEG}	+0.3 to -20	V
Max. drive voltage range	V_{POS}-V_{NEG}	40	V
Gate supply range	V_{GG}-V_{EE}	40	V
Operating temp. range		0 to +50	°C

Ta = 25 ± 2 ºC

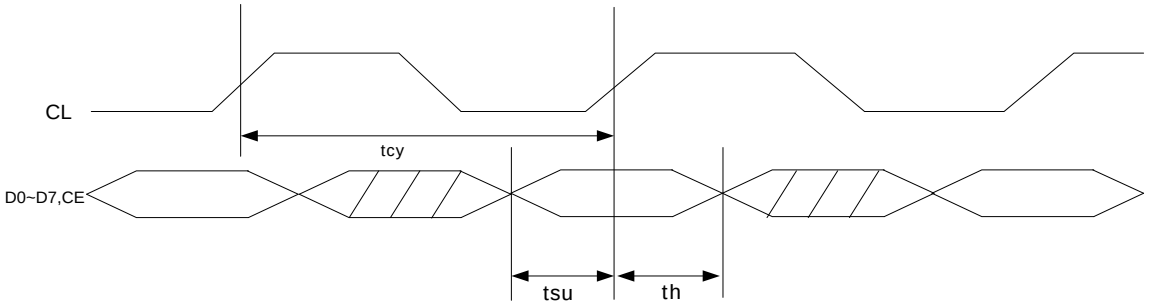
3.2 Recommended Operation Conditions of Panel

Table 3-2 Recommended Operation Conditions of Panel

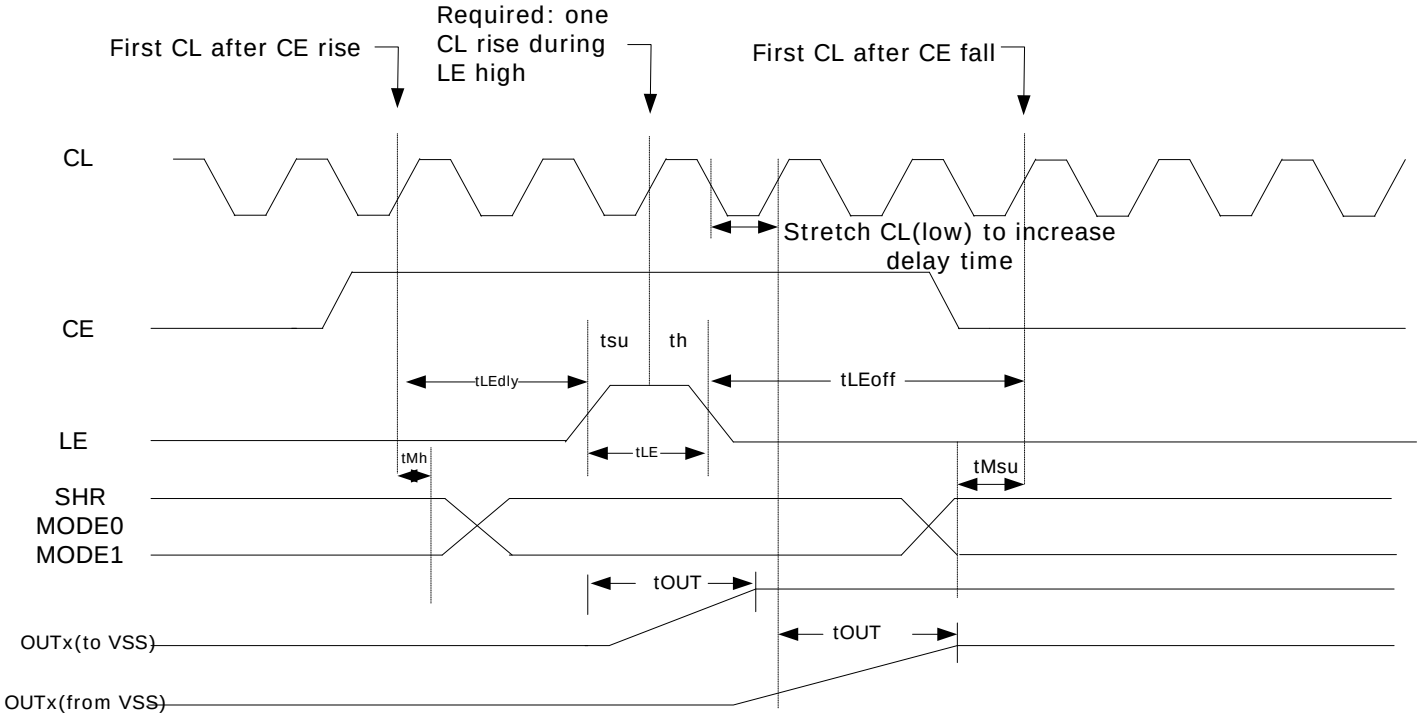
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Signal Ground	V_{SS}	-	0	-	V
Logic Power	V_{DD}	3.0	3.3	3.6	V
Source positive Voltage	V_{POS}	14	15	16	V
Source negative Voltage	V_{NEG}	-16	-15	-14	V
Gate positive Voltage	V_{GG}	V_{POS}+5	22	V_{EE}+40	V
Gate negative Voltage	V_{EE}	-21	-20	V_{NEG}-5	V
Common voltage	V_{COM}	-	-1.8	-	V

Ta = 25 ± 2 ºC

3.3 Source driver Ac characteristics

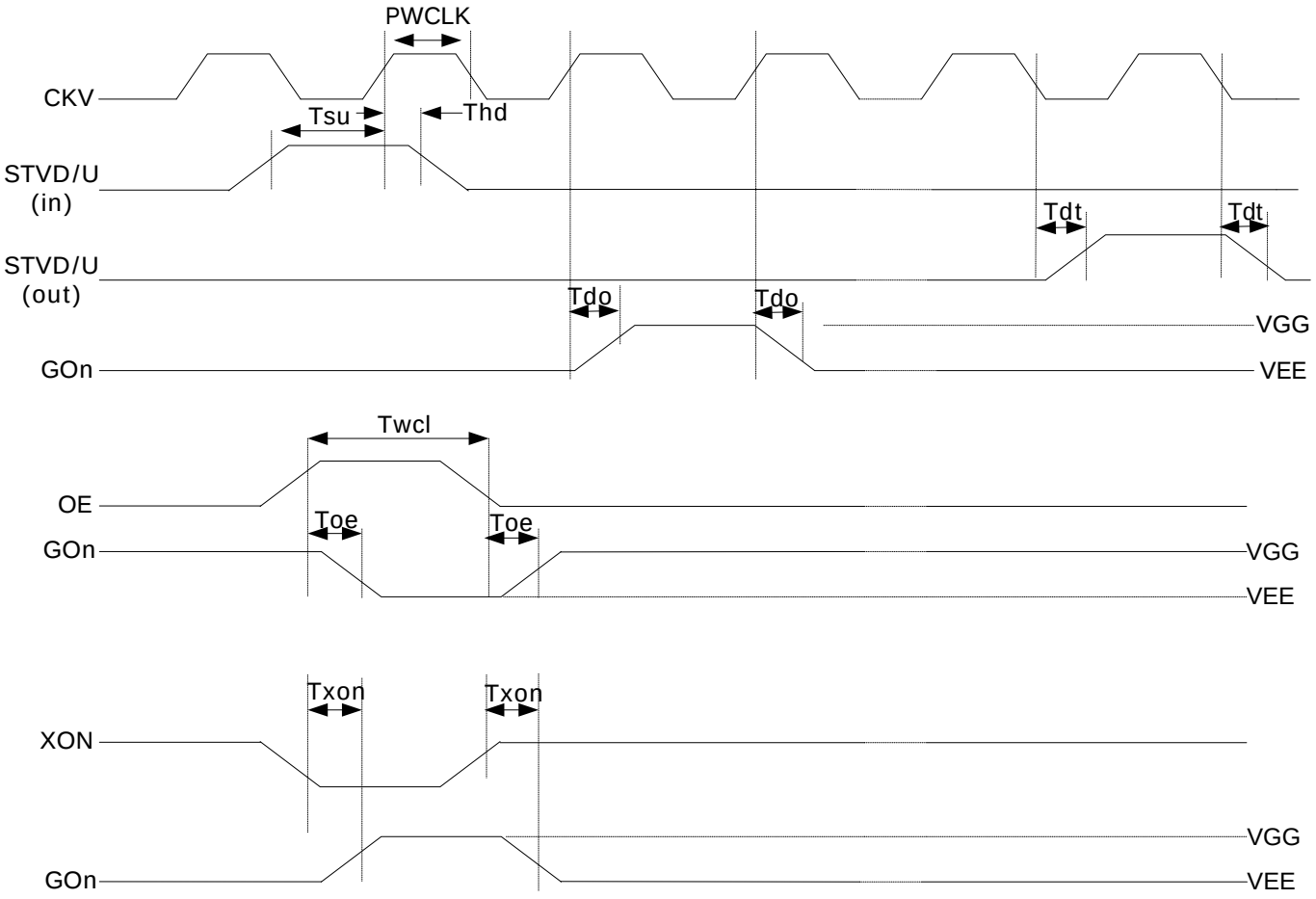


Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock CL cycle time	tcy	40	-	-	ns
D0...D7, CE setup time	tsu	8	-	-	ns
D0...D7, CE holt time	th	1	-	-	ns



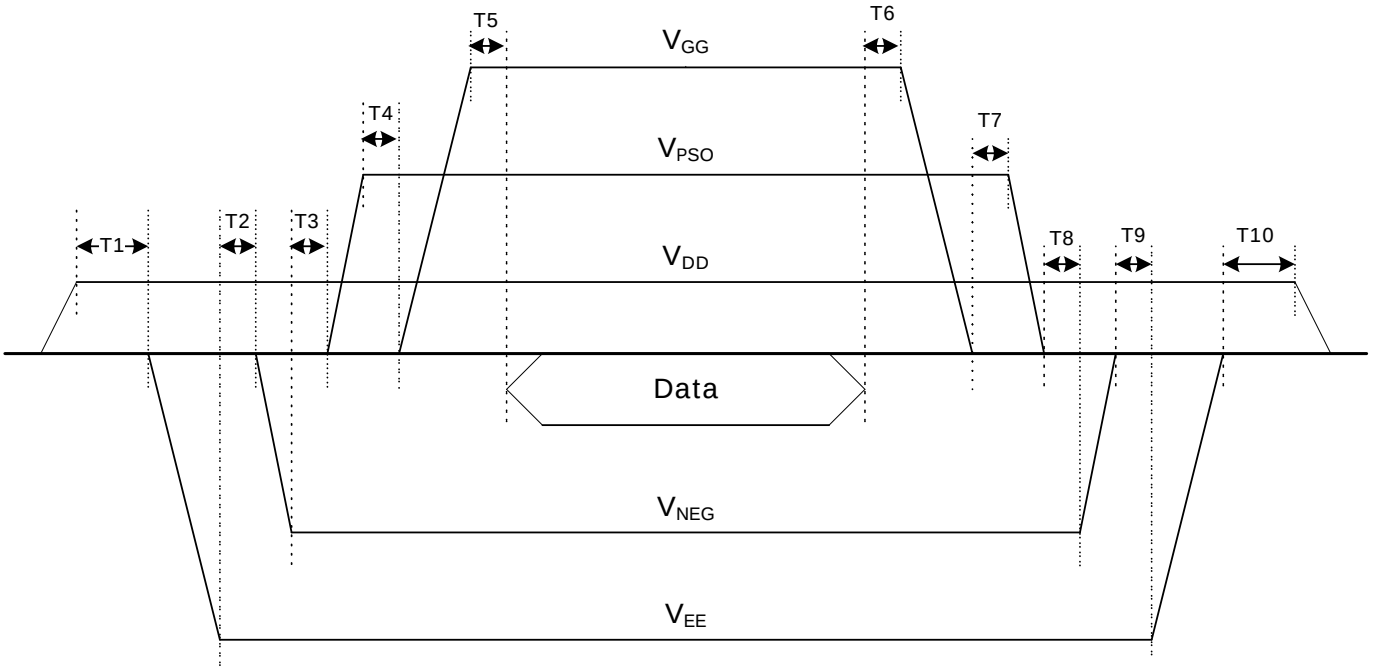
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
LE on delay time	tLEdly		40	-	-	ns
LE high-level pulse width	tLEw		40	-	-	ns
LE off delay time	tLEoff		40	-	-	ns
SHR,MODE0,MODE1 setup time	tMsu		100	-	-	ns
SHR,MODE0,MODE1 hold time	tMh		10	-	-	ns
Output settling time to +/-30mV	tOUT	Cload=50pf	100	-	12	us

3.4 Gate driver AC characteristics



Parameter	Symbol	Condition.	Min.	Typ.	Max.	Unit
Clock pulse width(High to low period)	PWCLK		500			ns
STVD/STVU setup time	Tsu		200			ns
STVD/STVU hold time	Thd		300			ns
Driver output delay time	Tdo	CL=220pF			900	ns
STVD/STVU delay time	Tdt	CL=220pF			500	ns
Output enable pulse width	Twcl		1			us
OE to driver output delay time	Toe	CL=220pF			900	ns
XON to driver output delay time	Txon	CL=220pF			10	us

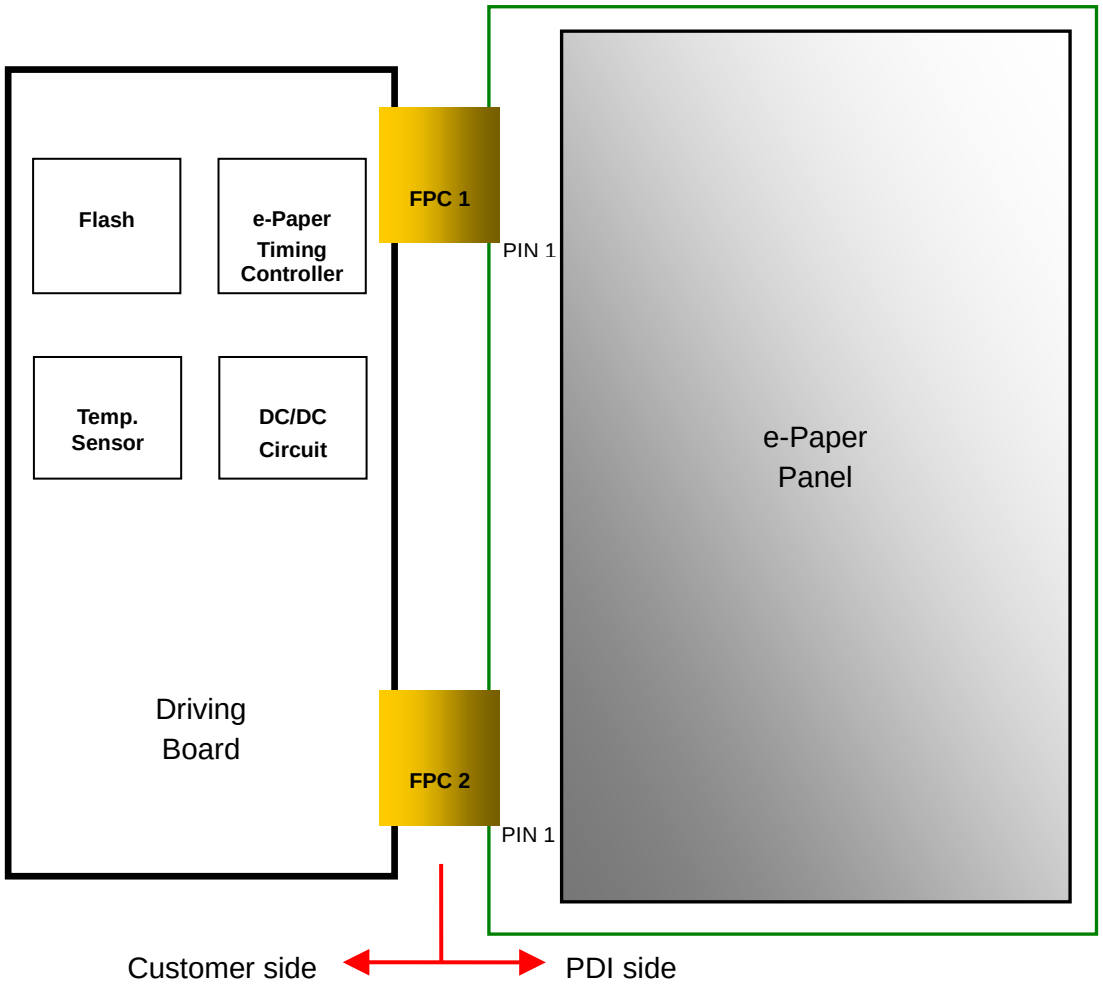
3.5 Power ON / OFF sequence



Symbol	Min.	Max.
T1	20 ms	-
T2	4 ms	-
T3	4 ms	-
T4	4 ms	-
T5	100 us	-
T6	100 us	-
T7	4ms	-
T8	4ms	-
T9	4ms	-
T10	20ms	-

4 Application Circuit Block Diagram

Figure 4-1 Application Circuit Block Diagram



5 Panel Pin Assignment

5.1 Terminal Pin Assignment

Table 5-1 FPC1 Pin Assignment

No.	Signal	Type	Connected to	Function
1	DUMMY	-	Floating	Dummy pin
2	GND	P	Ground	Grounding
3	V_{DD}	P	V_{DD}	Logic power supply
4	V_{GG}	P	V_{GG}	Gate driver positive power supply
5	V_{EE}	P	V_{EE}	Gate driver negative power supply
6	STVD	I/O	MCU / Floating	Gate start pulse. When U/D=1, the pin is input.
7	CKV	I	MCU	Line clock
8	U/D	I	MCU	Gate scan direction
9	OE123	I	MCU	Output enable 1, 2 and 3 (connected)
10	XON	I	V_{CC}	When XON goes low, all outputs are fixed to V_{GG}
11	VST	P	V_{COM}	Common voltage (capacitor line)
12	BORDER	P	Border control circuit	Border area power supply
13	V_{COM}	P	V_{COM}	Common voltage (backplane)
14	DUMMY	-	Floating	Dummy pin
15	DUMMY	-	Floating	Dummy pin
16	DUMMY	-	Floating	Dummy pin
17	V_{NEG}	P	V_{NEG}	Source driver negative power supply
18	V_{POS}	P	V_{POS}	Source driver positive power supply
19	V_{DD}	P	V_{DD}	Logic power supply
20	CKH	I	MCU	Source driver clock
21	GND	P	Ground	Grounding

No.	Signal	Type	Connected to	Function
22	D0_O	I	MCU	Bit0 of the Odd data bus
23	D1_O	I	MCU	Bit1 of the Odd data bus
24	D2_O	I	MCU	Bit2 of the Odd data bus
25	D3_O	I	MCU	Bit3 of the Odd data bus
26	D4_O	I	MCU	Bit4 of the Odd data bus
27	D5_O	I	MCU	Bit5 of the Odd data bus
28	D6_O	I	MCU	Bit6 of the Odd data bus
29	D7_O	I	MCU	Bit7 of the Odd data bus
30	CE	I	MCU	Source driver chip enable
31	LE	I	MCU	Source driver latch enable
32	OE	I	MCU	Source driver output enable
33	SHR_O	I	Ground	Source scan direction
34	GND	P	Ground	Grounding
35	V_{DD}	P	V_{DD}	Logic power supply
36	V_{POS}	P	V_{POS}	Source positive power supply
37	V_{NEG}	P	V_{NEG}	Source negative power supply
38	BORDER	P	Border control circuit	Border area power supply
39	VST	P	V_{COM}	Common voltage (capacitor line)
40	DUMMY	-	Floating	Dummy pin

Table 5-2 FPC2 Pin Assignment

No.	Signal	Type	Connected to	Function
1	DUMMY	-	Floating	Dummy pin
2	VST	P	V_{COM}	Common voltage (capacitor line)
3	BORDER	P	Border control circuit	Border area power supply
4	V_{NEG}	P	V_{NEG}	Source driver negative power supply
5	V_{POS}	P	V_{POS}	Source driver positive power supply
6	V_{DD}	P	V_{DD}	Logic power supply
7	CKH	I	MCU	Source driver clock
8	GND	P	Ground	Grounding
9	D0_E	I	MCU	Bit0 of the Even data bus
10	D1_E	I	MCU	Bit1 of the Even data bus
11	D2_E	I	MCU	Bit2 of the Even data bus
12	D3_E	I	MCU	Bit3 of the Even data bus
13	D4_E	I	MCU	Bit4 of the Even data bus
14	D5_E	I	MCU	Bit5 of the Even data bus
15	D6_E	I	MCU	Bit6 of the Even data bus
16	D7_E	I	MCU	Bit7 of the Even data bus
17	CE	I	MCU	Source driver chip enable
18	LE	I	MCU	Source driver latch enable
19	OE	I	MCU	Source driver output enable
20	SHR_E	I	V_{DD}	Source scan direction
21	GND	P	Ground	Grounding
22	V_{DD}	P	V_{DD}	Logic power supply
23	V_{POS}	P	V_{POS}	Source positive power supply
24	V_{NEG}	P	V_{NEG}	Source negative power supply

No.	Signal	Type	Connected to	Function
25	DUMMY	-	Floating	Dummy pin
26	DUMMY	-	Floating	Dummy pin
27	DUMMY	-	Floating	Dummy pin
28	V_{COM}	P	V_{COM}	Common voltage (backplane)
29	BORDER	P	Border control circuit	Border area power supply
30	VST	P	V_{COM}	Common voltage (capacitor line)
31	XON	I	V_{CC}	When XON goes low, all outputs are fixed to V_{GG}
32	OE123	I	MCU	Output enable 1, 2 and 3 (connected)
33	U/D	I	MCU	Gate scan direction
34	CKV	I	MCU	Line clock
35	STVU	I/O	MCU / Floating	Gate start pulse. When U/D=0, the pin is input.
36	V_{EE}	P	V_{EE}	Gate driver negative power supply
37	V_{GG}	P	V_{GG}	Gate driver positive power supply
38	V_{DD}	P	V_{DD}	Logic power supply
39	GND	P	Ground	Grounding
40	DUMMY	-	Floating	Dummy pin

Note:

I: Input
O: Output
P: Power

6 Optical Characteristics

6.1 Test Conditions

Table 6-1 Optical Test Conditions

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	ºC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC} & V_{DD}	3.3	V

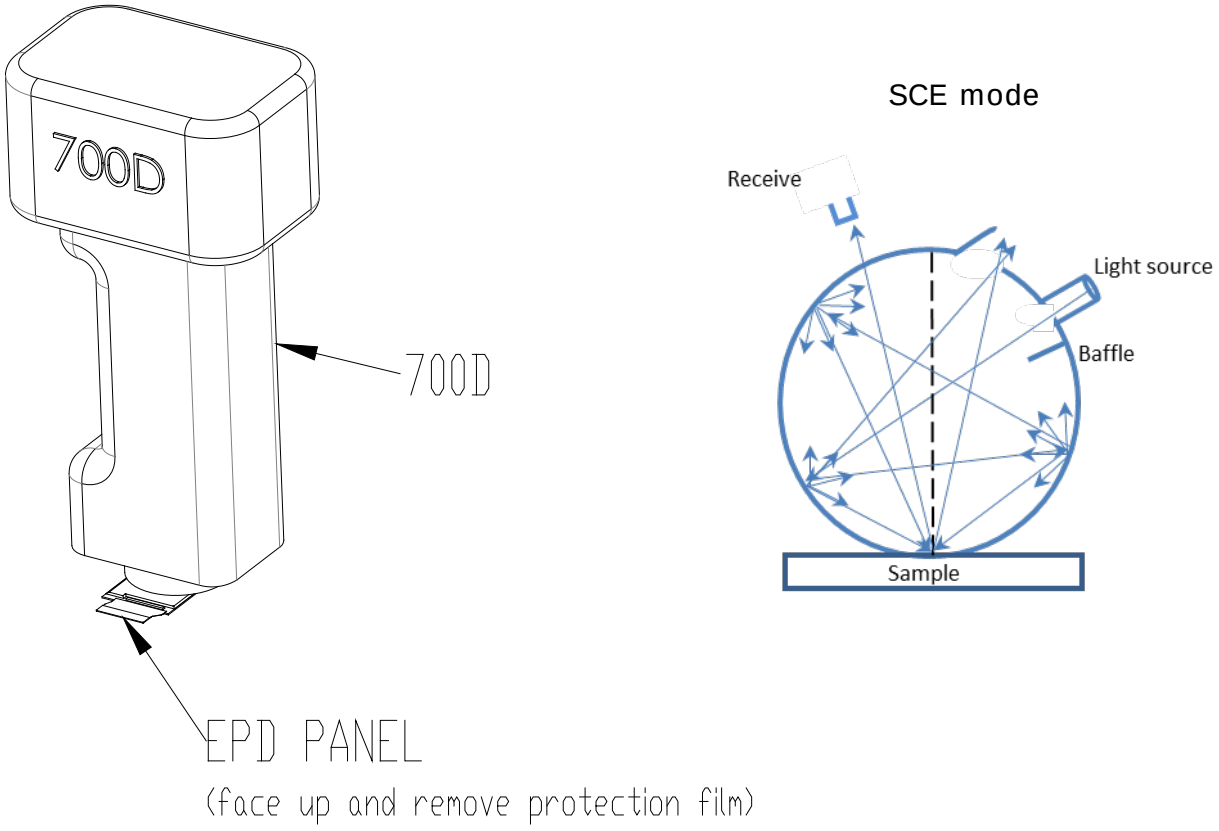
6.2 Optical Specifications

Table 6-2 Optical Measurement with D65 light source

Item	Symbol	Rating			Unit	Note
		Min.	Typ.	Max.		
Contrast ratio	CR	-	7:1	-	-	θx=θy=0 (1),(2),(3),(4)
Refresh time	Tr	-	3.2	-	sec	(3)
White Chromaticity	Wx	-	0.30	-	-	θx=θy=0 (1),(4)
	Wy	-	0.33	-		
Reflectance	R%	-	32	-	%	(1),(4)

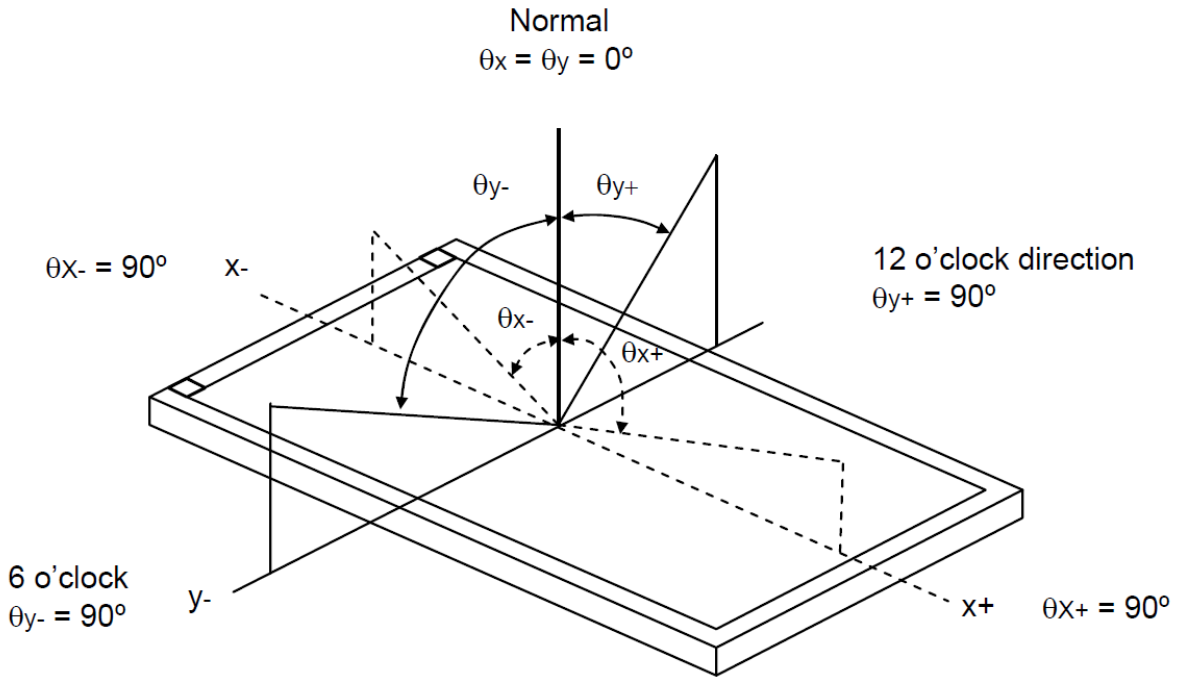
Note (1): Panel is driven by PDI waveform without masking film and optical measurement by CM-700D with D65 light source and SCE mode.

Figure 6-1 The optical measurement by CM-700D with D65 light source and SCE mode



Note (2): Definition of Viewing Angle (θx, θy):

Figure 6-2 Definition of Viewing Angle to Measure Contrast Ratio



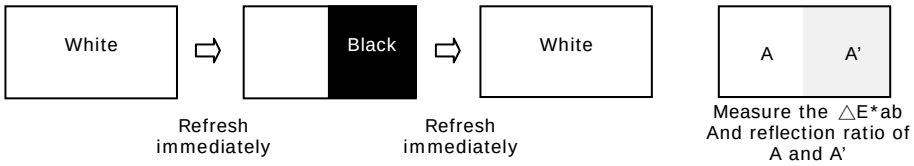
Note (3): Refresh time is the time that e-paper particles move not including the power on and off time. The refresh time is measured at 25°C.The refresh time and contrast ratio varies due to different films, display performance requirements, and ambient temperatures.

Note (4): Contrast ratio (C.R.): The Contrast ratio is calculated by the following expression. C.R. =(R% White) / (R% Black). Reflectance is measured at 120 seconds after refresh.

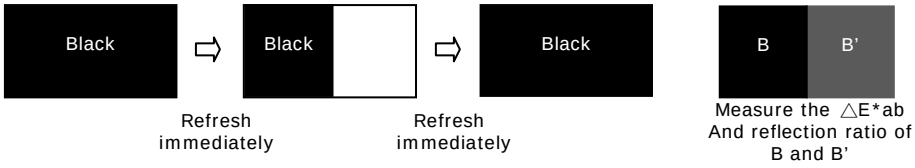
6.3 Ghosting

Below are two test methods to verify that ghosting within an acceptable range. Test 1 and Test 2 use measured data to calculate Delta E which is a single number representing the distance between two colors in a 3 dimensional color space. Test 1 and Test 2 are performed at 25ºC.

- Test 1: White to Black Ghosting



- Test 2: Black to White Ghosting



The formula is used to calculate Test1 and Test2. For example of Test 2:

$$\Delta E^*ab = [\ (L_B - L_{B'})^2 + (a_B - a_{B'})^2 + (b_B - b_{B'})^2\ ]^{1/2}$$

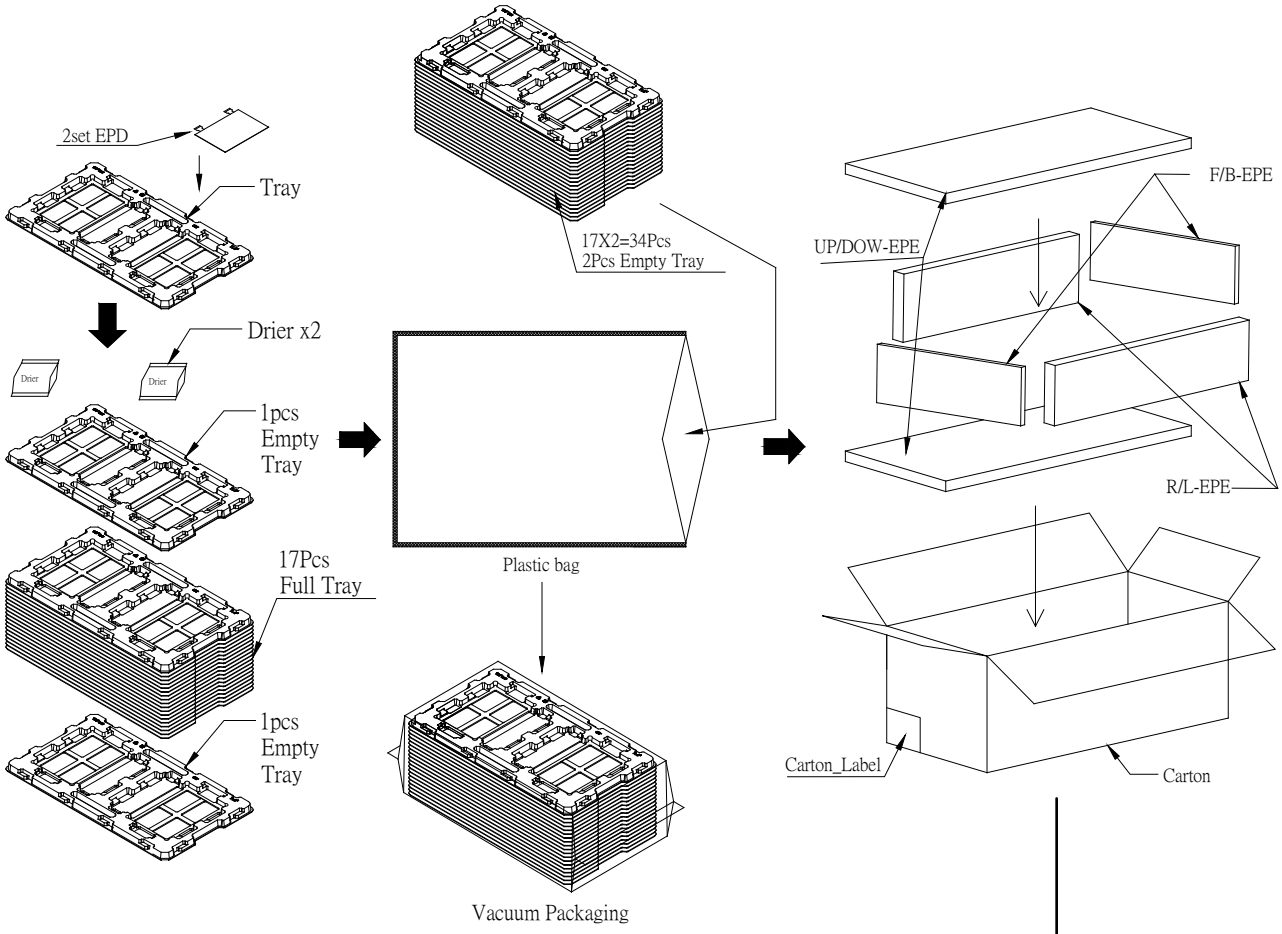
Table 6-3 Measurement of Ghosting

Item	Rating		
	Min.	Typ.	Max.
Test 1 △E*ab	-	-	2
Test 2 △E*ab	-	-	2

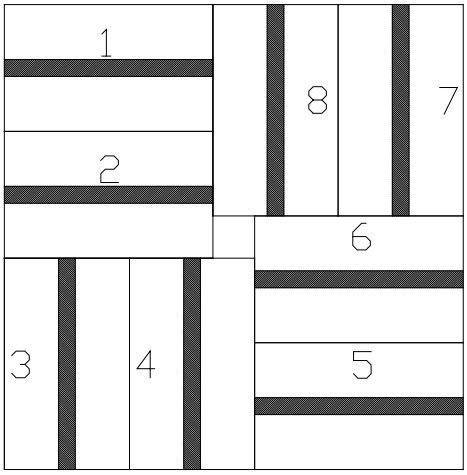
Note: Panel is driven by PDI waveform without masking film and optical is measured by CM-700D with D65 light source and SCE mode.

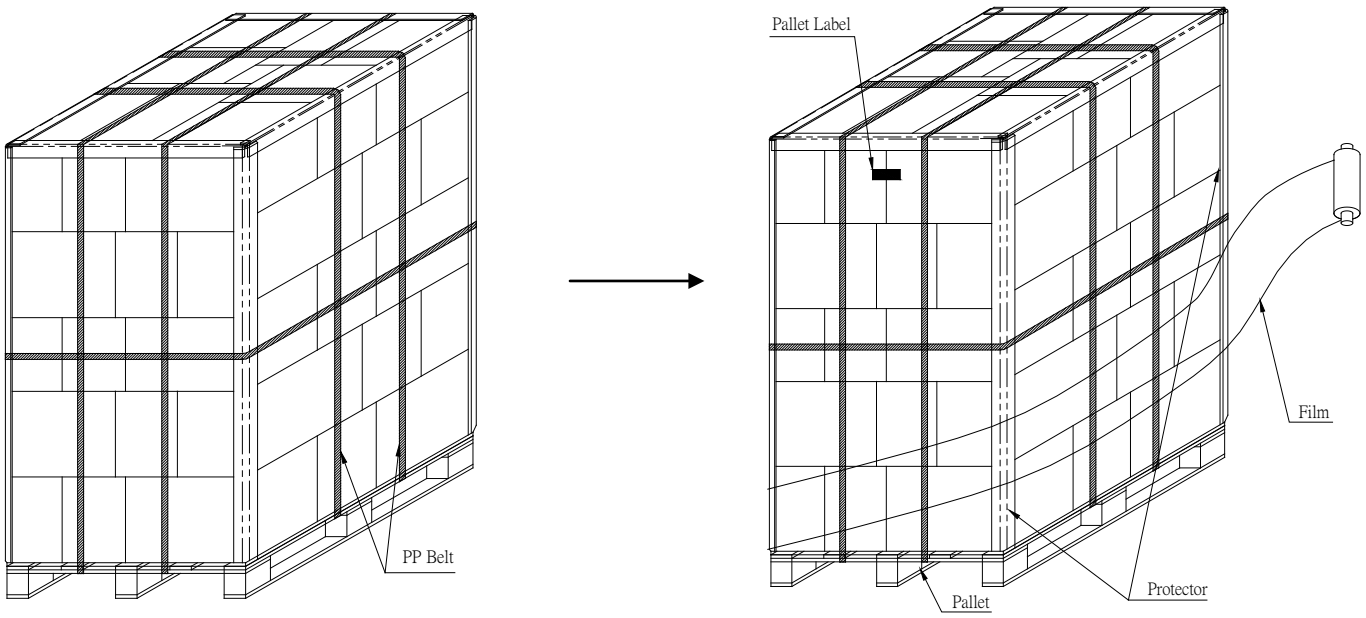
7 Packing

Figure 7-1 Packing Diagram



Note: 1.Carton outline size: 500L X 300W X 200H mm
2.Material of tray: A-PET
3.Material of plastic bag: PE-LD

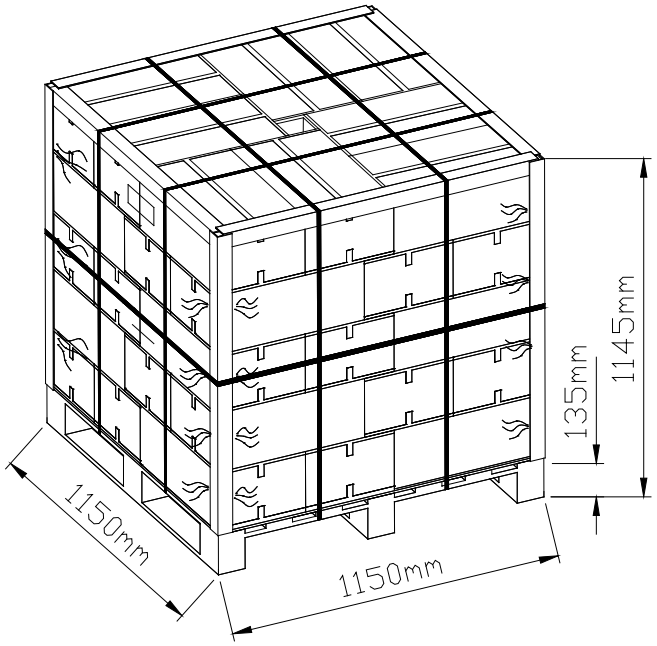




34(pcs)x40(BOX)=1360pcs

	7.4” EPD BOX
N.W. :	1.49 Kg
G.W. :	4.8 Kg

Sea / Land / Air Transportation



8 Precautions

(1) The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel.

(2) It is recommended to assemble or install EPD panels in a clean working area. Dust and oil may cause electrical shorts or degrade / scratch / den the protection sheet film.

(3) Do not apply pressure to the EPD panel in order to prevent damaging it.

(4) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(5) Please support the bezel with your finger while connecting the interface cable such as the FPC.

(6) Do not stack the EPD panels / Modules.

(7) Do not press the FPC on the glass edge or Pull FPC up / down to 90°.

(8) Do not touch the FPC lead connector.

(9) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(10) Wear a Wrist Strap (Grounding connect) when handling and during assembly. Semiconductor devices are included in the EPD Panel / Module and they should be handled with care to prevent any electrostatic discharge (ESD). (An Ion Fan may be needed in assembly operation to reduce ESD risk.)

(11) Keep the EPD Panel / Module in the specified environment and original packing boxes when storage in order to avoid scratching and keep original performance.

(12) Do not disassemble or reassemble the EPD panel.

(13) Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating. This behavior would make dent or scratch on protection sheet.

(14) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(15) It's low temperature operation product. Please be mindful the temperature different to make frost or dew on the surface of EPD panel. Moisture may penetrate into the EPD panel because of frost or dew on surface of EPD panel, and makes EPD panel damage.

(16) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time. Please store the EPD panel in controllable environment of warehouse and original package: Without sunlight, without condensation, a temperature range of 15ºC to 35ºC, and humidity from 30%RH to 60%RH.

(17) The label ink used for marking the Panel ID number is erased easily by solvent. Please avoid using solvent to clean the EPD panel.

(18) The EPD is vacuum packed.

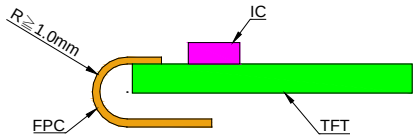
(19) Before approved by PDI and customer, products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.

(20) PDI makes every attempt to ensure that its products are of high quality and reliability. However, contact PDI sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.

(21) Design your application so that the product is used within the ranges guaranteed by PDI particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. PDI bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail safes, so that the equipment incorporating PDI product does not cause bodily injury, fire or other consequential damage due to operation of the PDI product.

(22) This product is not designed to be radiation resistant.

(23) Please keep R≧1.0mm when bend for assembly.



9 Definition of Labels

Figure 9-1 Model Labels

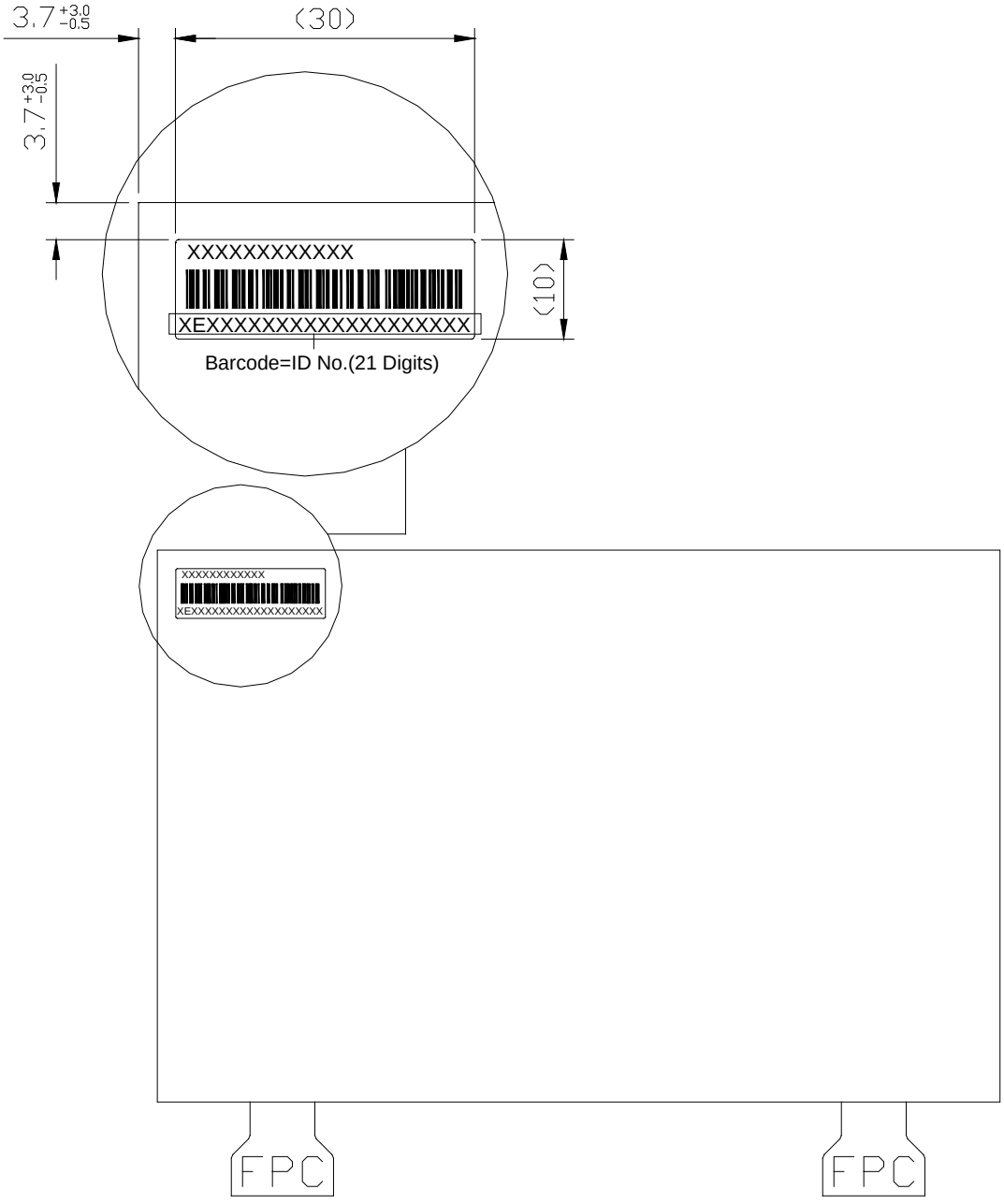


Figure 9-2 Definition of Model Labels

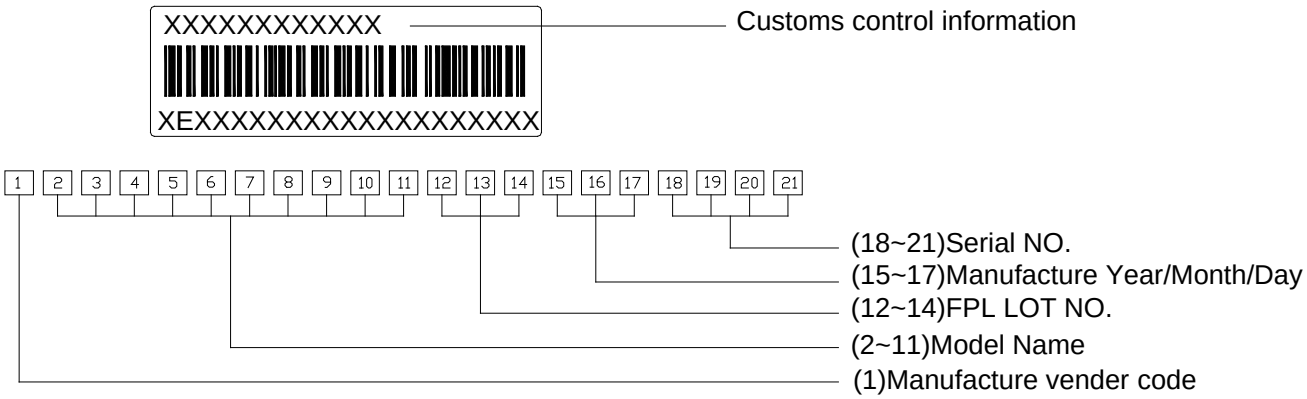
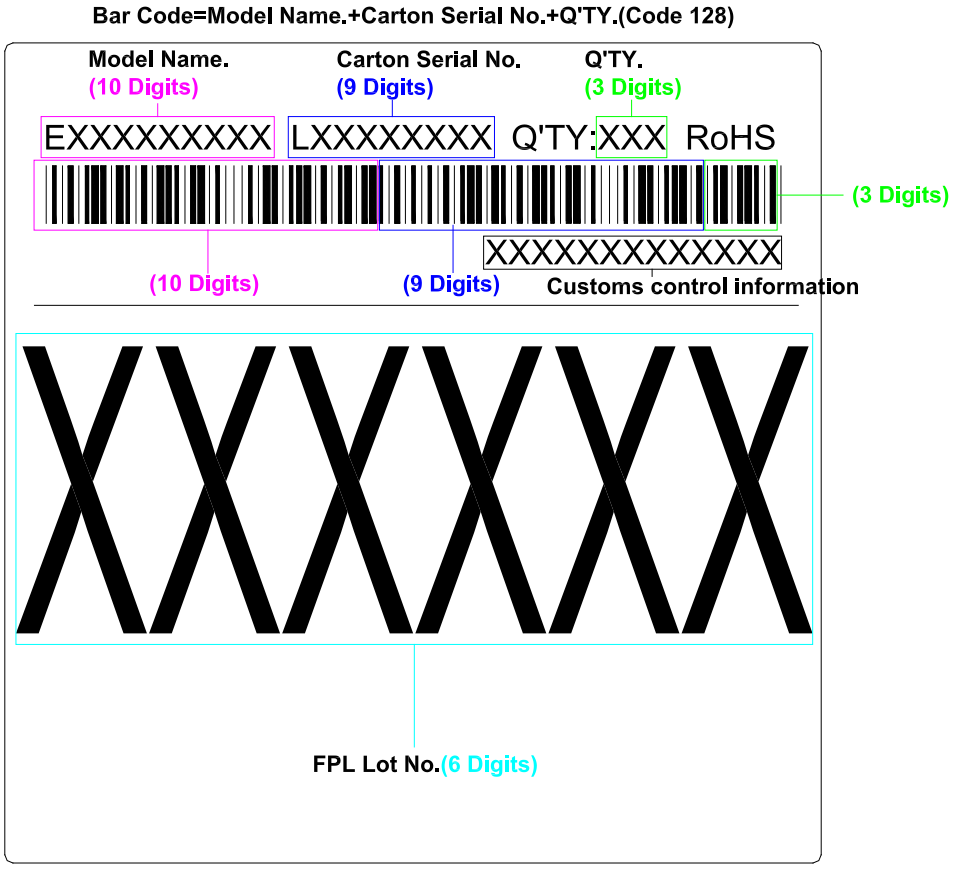
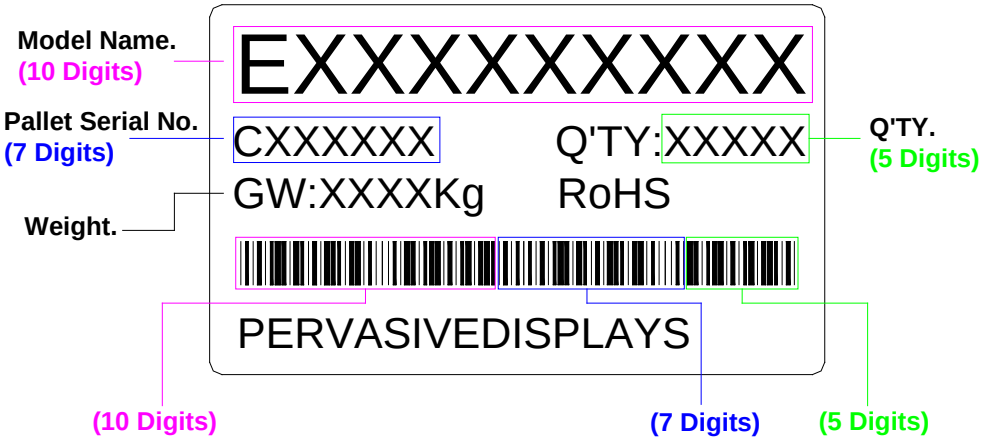


Figure 9-3 Carton Label



Carton Label

Figure 9-4 Pallet Label



Bar Code=Model Name.+Pallet Serial No.+Q'TY.(22 Digits)

Pallet Label