

Application Note

for

2.7" Monochrome EPD

(OTP LUT and Fast update)

Description	Interface for 2.7" Mono EPD. Using embedded OTP LUT supports Fast update.
Model Name	E2271PS09x
Date	2021/5/27
Doc. No.	
Revision	03

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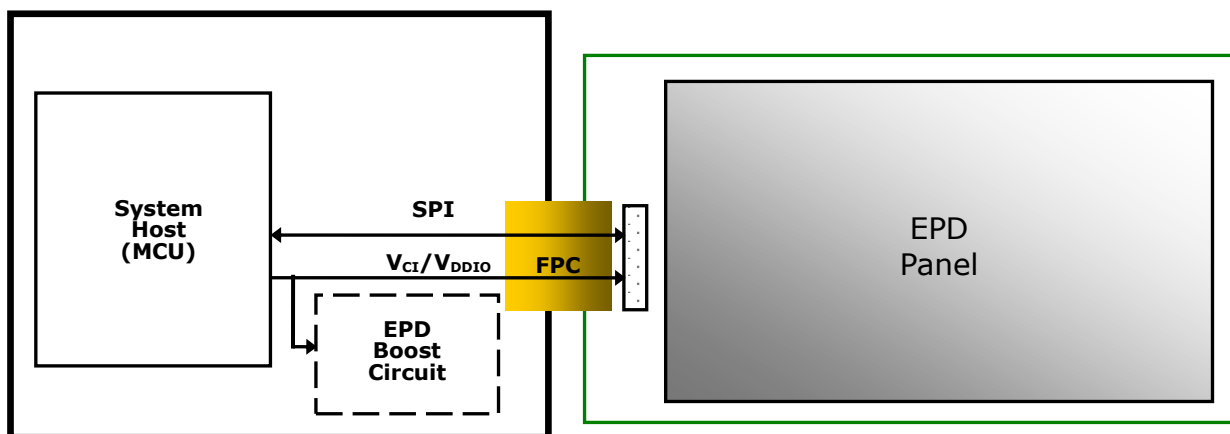
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1. General Description

1.1 Overview

The document introduces how to drive the 2.7" EPD with OTP LUT. The EPD has supported the Fast update and equipped the function of the partial window update. The EPD use single driver and that embedded T-con. The major control interface of the driver is SPI. The host sends both the setting commands and the display image to driver through the SPI bus.



1.2 Definition of operation mode

The section will define and clarify several update modes, their names are easy to confuse.

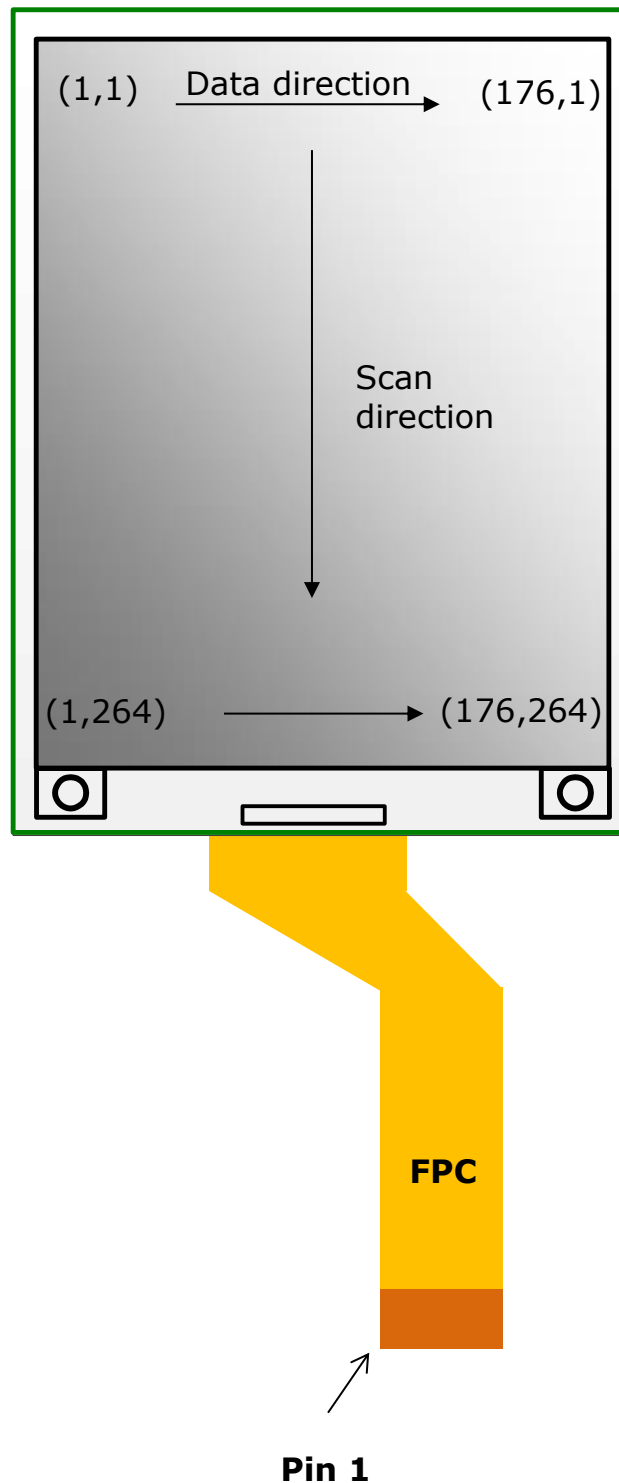
Normal update: it will perform the complete waveform for image update. The process will go through the inverse, shaking and imaging phases. The mode will take more time, but it will bring better image performance.

Fast update: the short waveform will be executed. COG compares the pixel data of the current image and the new image pixel by pixel, and then only drives the transition pixels. The mode can quickly complete the image update.

Partial update: user can set the update window range and only send the image data of the window area. If the user only needs to change a small part of the display, this function can reduce the amount of inputting image data.

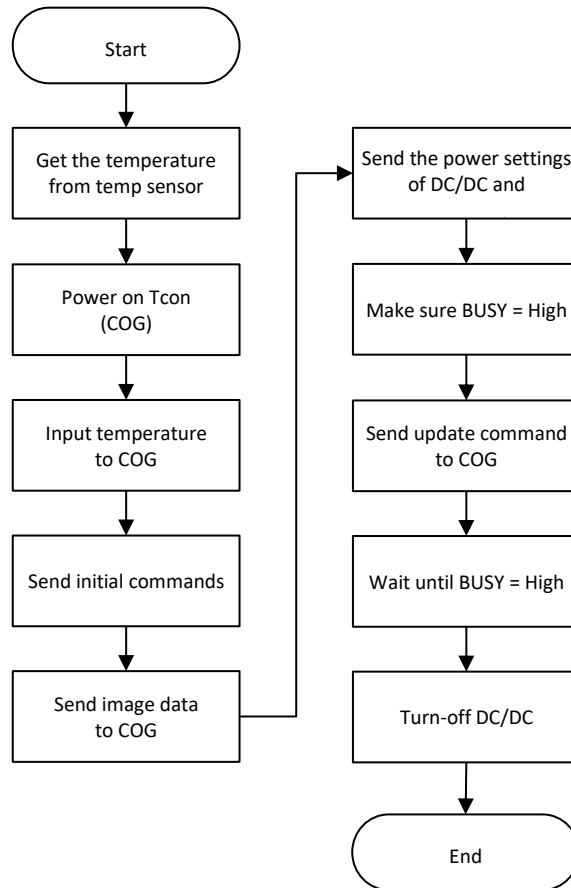
1.3 Panel drawing

2.7-inch EPD



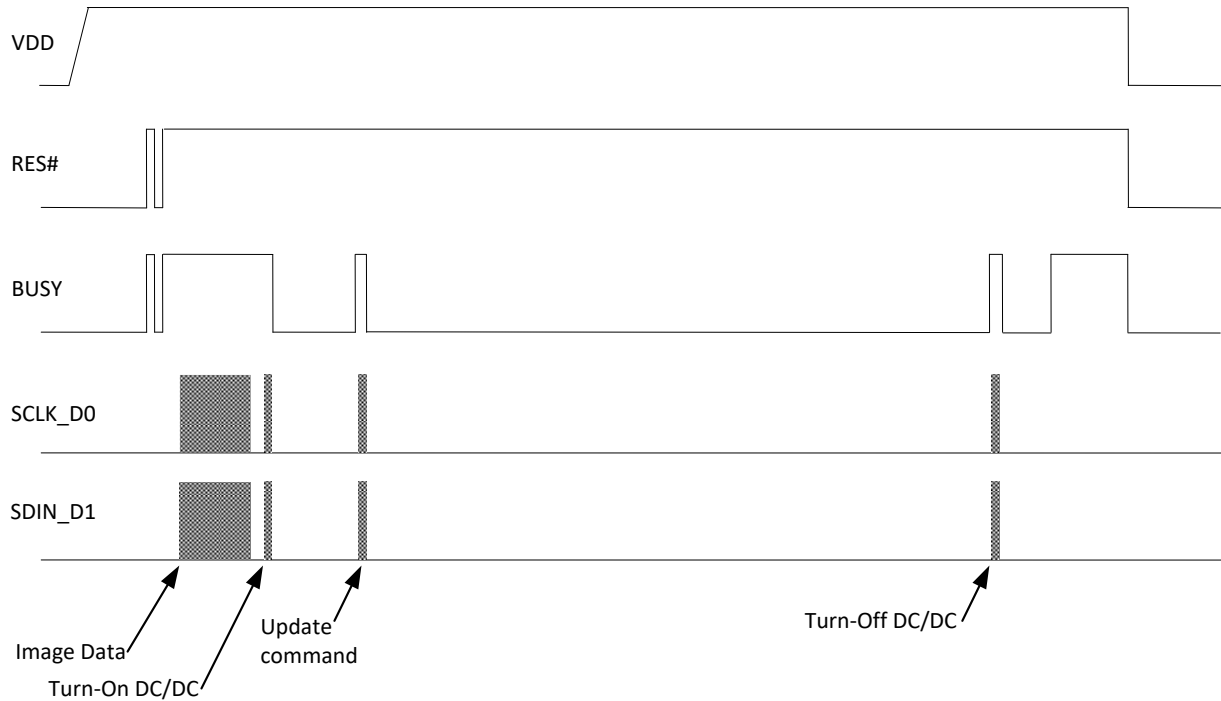
1.4 EPD Driving Flow Chart

The flowchart below provides an overview of the necessary actions to update the EPD. The steps below refer to the detailed descriptions in the respective sections.



1.5 Overall Waveform

The diagram below provides a signal control overview during an EPD update cycle.



1.6 SPI Timing Format

SPI commands are used to communicate between the MCU and the COG Driver. The SPI format used differs from the standard in that two-way communications are not used, and CS is pulled high then low between clocks. When setting up the SPI timing, PDI recommends verify both the SPI command format and SPI command timing in this section.

- Below is a description of the SPI Format:

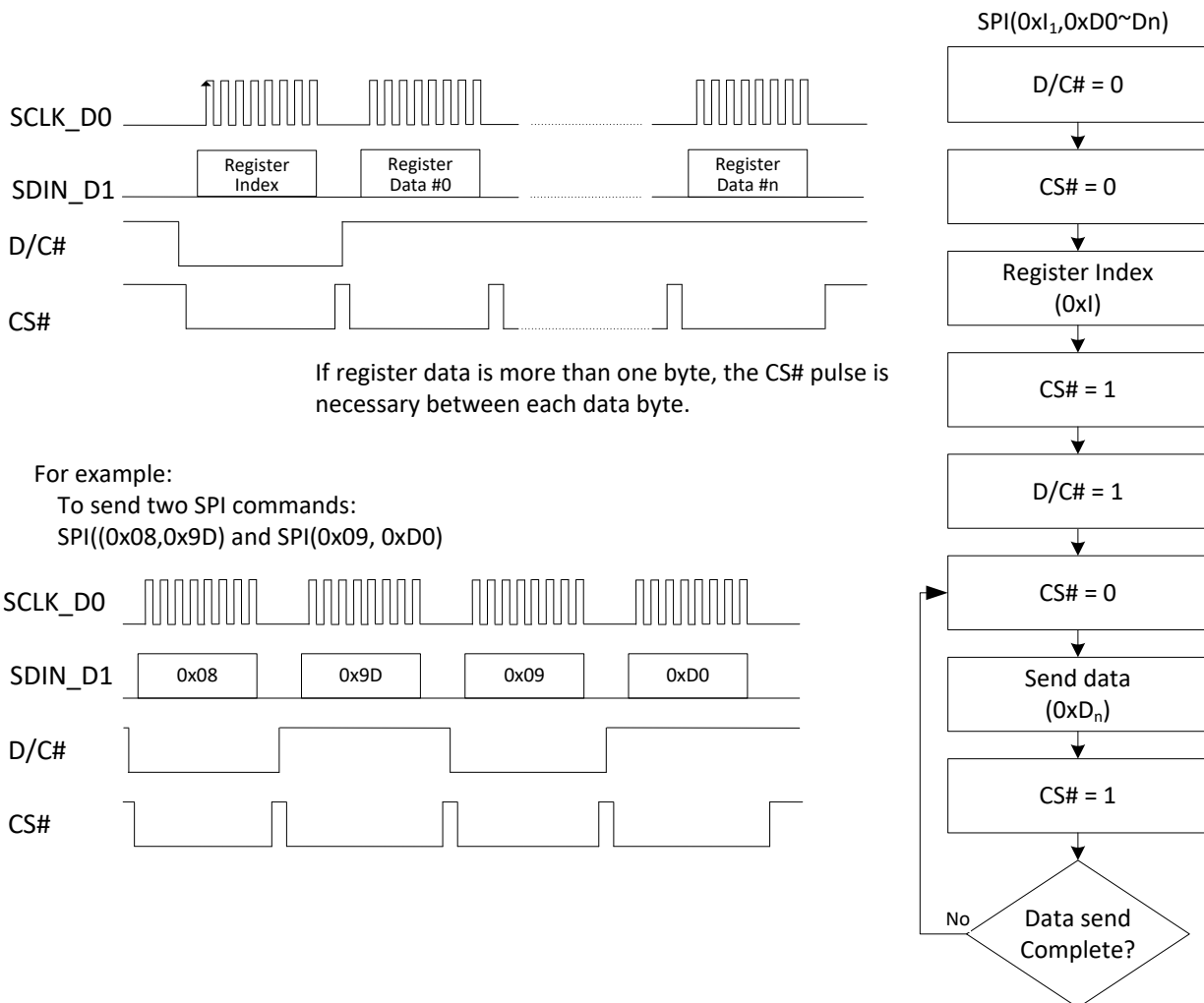
SPI(0xI, 0xD0, 0xD1, 0xD2, ...)

Where:

I is the Register Index and the length is 1 byte

D0~n is the Register Data. The Data length is variable by different Register Index.

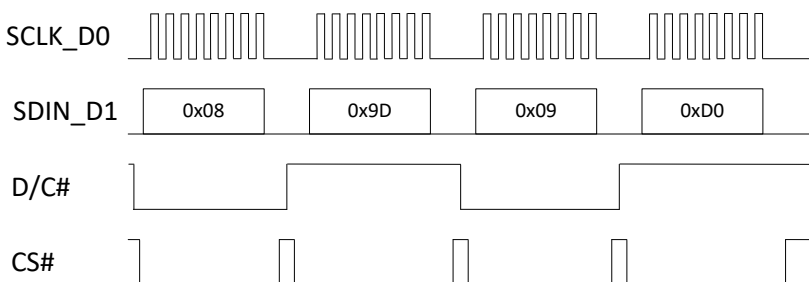
- SPI command signals and flowchart:



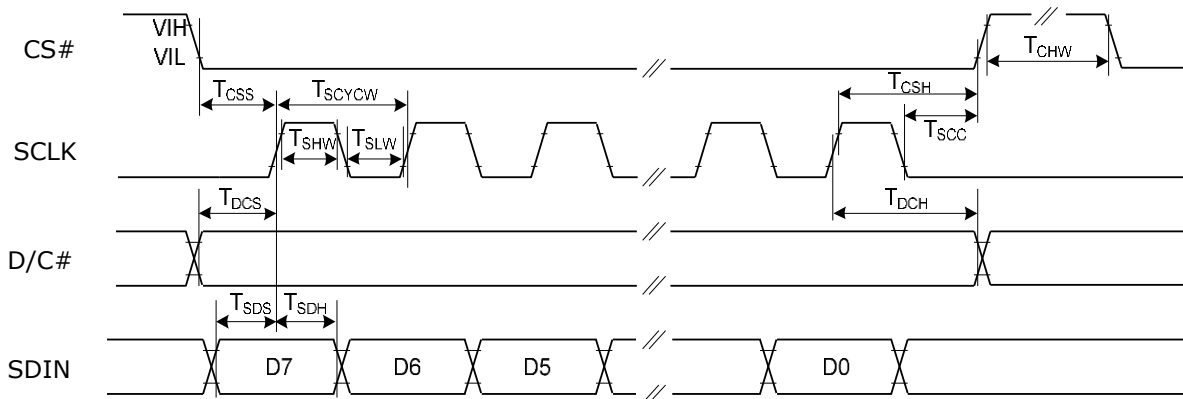
For example:

To send two SPI commands:

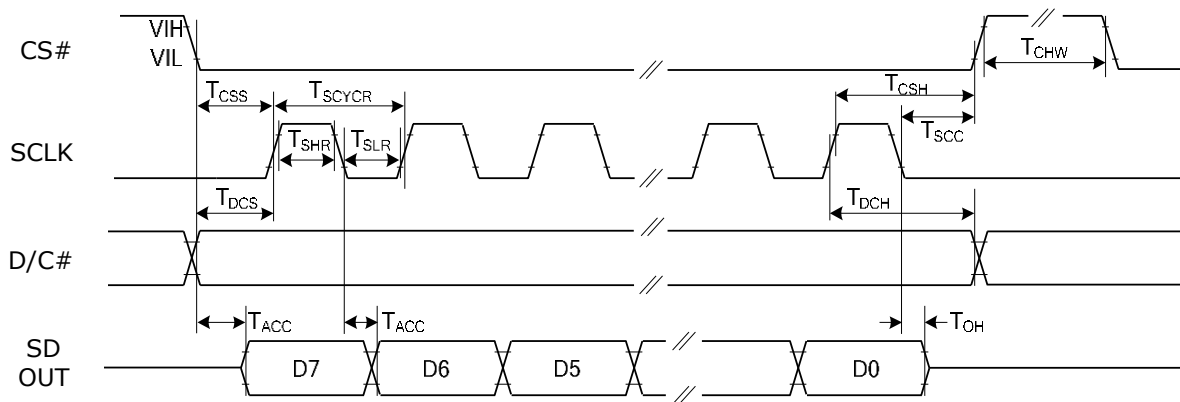
SPI((0x08,0x9D) and SPI(0x09, 0xD0)



• SPI command timing



Write mode

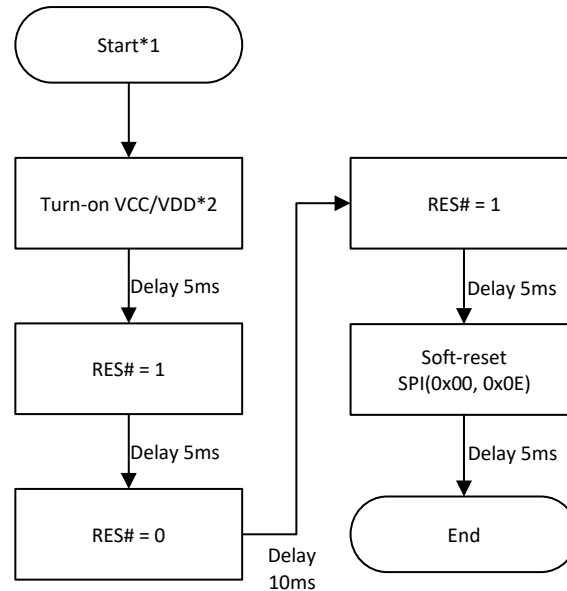


Read mode

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Chip Select Setup Time	t_{CSS}	60	-	-	ns	
Chip Select Hold Time	t_{CSH}	65	-	-	ns	
Chip Select Setup Time	t_{SCH}	20	-	-	ns	
Chip Select Setup Time	t_{CHW}	40	-	-	ns	
Serial Clock Cycle (Write)	t_{SCYCW}	100	-	-	ns	
SCLK "H" Pulse Width (Write)	t_{SHW}	35	-	-	ns	
SCLK "L" Pulse Width (Write)	t_{SLW}	35	-	-	ns	
Serial Clock Cycle (Read)	t_{SCYCR}	150	-	-	ns	
SCLK "H" Pulse Width (Read)	t_{SHR}	60	-	-	ns	
SCLK "L" Pulse Width (Read)	t_{SLR}	60	-	-	ns	
DC Setup Time	t_{DCS}	30	-	-	ns	
DC Hold Time	t_{DCH}	30	-	-	ns	
Data Setup Time	t_{SDS}	30	-	-	ns	
Data Hold Time	t_{SDH}	30	-	-	ns	
Access Time	t_{ACC}	-	-	50	ns	
Output Disable Time	t_{OH}	15	-	-	ns	

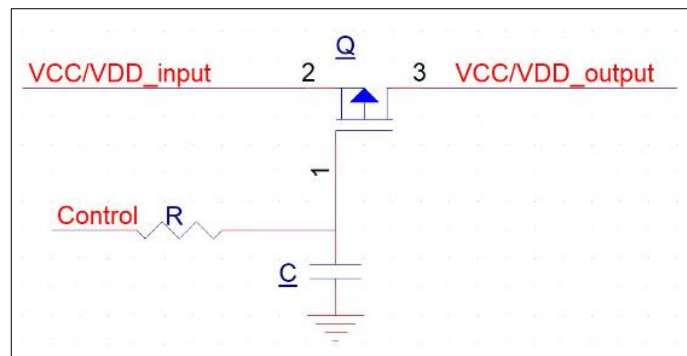
2. Power on COG driver

This flowchart describes power sequence for driver chip.



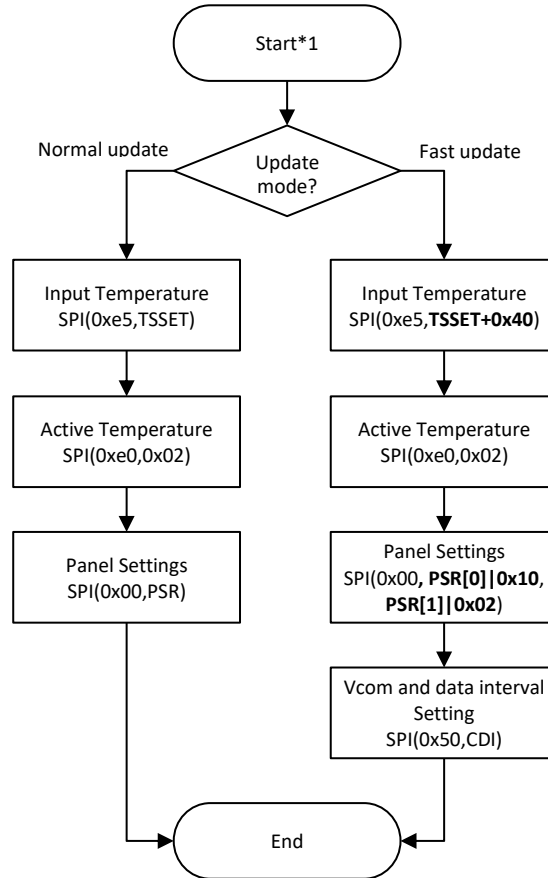
Note:

1. Start: initial state the VCC/VDD, RES#, CS#, SDIN, SCLK = 0
2. In order to the inrush current will case other issue. It is recommended to add soft-start when VCC/VDD is turned on. (as the circuit below)



3. Input initial command

Please send the initial command to EPD according to the flowchart.



Note:

1. Start: Follow the end of the power on sequence.

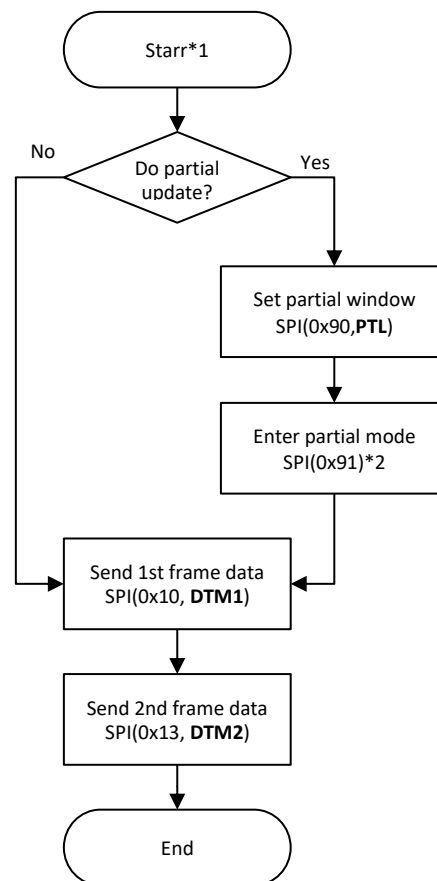
TSSET: is the temperature value and unit are degree of Celsius. The maximum and minimum values of the TSSET are 50 and 0, respectively. If the actual temperature is out of the range, just set it to 50 or 0.

PSR: there are 2 bytes' data that must be read out from **0x4B** and **0x4C** of OTP memory.

CDI: this is a constant value of 0x07.

4. Input image to the EPD

This section describes how to send the image data into the COG driver. EPD needs to receive two frames image data each update but the image data definitions of "Normal" update and "Fast" update are different. The two frames image data must be sent into EPD from register of **0x10** and **0x13** respectively. The EPD equipped partial update function that allows user can only sends a small area data into COG for changing particular small area image.



Note:

1. Start: Follow the end of the initial command.
2. This register does not have data, just send the index. Once entering the partial mode, the exit partial mode command must be sent after finishing DRF (display refresh).

PTL: there are 7 bytes' data, the table is its layout of data

		D7	D6	D5	D4	D3	D2	D1	D0	
PTL	byte 0	HRST					0	0	0	
	byte 1	HRED					1	1	1	
	byte 2	0	0	0	0	0	0	0	VRST[8]	
	byte 3	VRST[7:0]								
	byte 4	0	0	0	0	0	0	0	VRED[8]	
	byte 5	VRED[7:0]								
	byte 6	0	0	0	0	0	0	0	PT_SCAN	

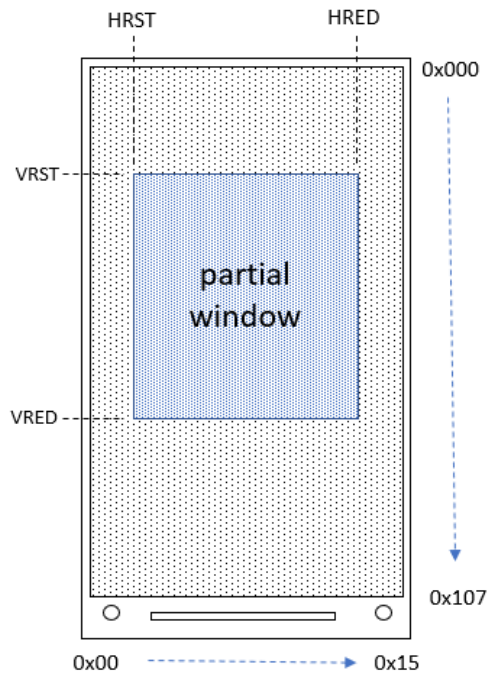
HRST: Horizontal start channel bank. A bank includes 8 pixels. The value range is from 0x00 to 0x15.

HRED: Horizontal end channel bank. A bank includes 8 pixels. The value range is from 0x00 to 0x15.

VRST: Vertical start line. The value range is from 0x000 to 0x107.

VRED: Vertical end line. The value range is from 0x000 to 0x107 but VRST must be greater than VRED.

PT_SCAN: this bit determines whether COG also scans the gate-channels that outside part of the partial window. PDI recommends setting this bit to the default value 1.



DTM1: the data is the image data. If the "partial window" is enable, the amount of image data is $(HRED - HRST + 1) \times (VRED - VRST + 1)$ bytes. If the "partial window" is disable, the amount is $0x108 \times 0x16$ bytes.

The data definition of DTM1 is different between "Normal update" and "Fast update".

Normal update: DTM1 image is the NEW image data that you want displaying next moment.

Fast update: DTM1 image is the OLD image data that already displayed on the EPD.

Data	Pixel Color
1	Black
0	White

DTM2: the data is the image data. If the "partial window" is enable, the amount of image data is $(HRED - HRST + 1) \times (VRED - VRST + 1)$ bytes. If the "partial window" is disable, the amount is $0x108 \times 0x16$ bytes.

The data definition of DTM2 is different between "Normal update" and "Fast update".

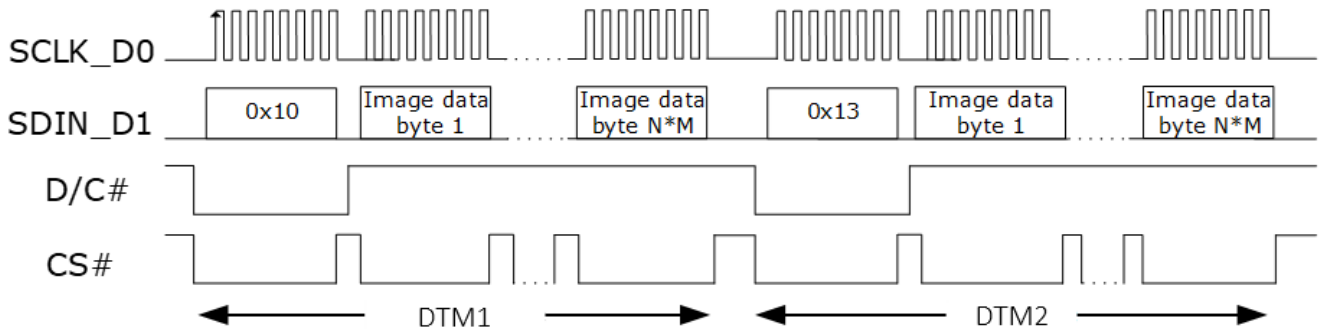
Normal update: DTM2 image is dummy data. It just needs to be filled with the enough amount of $0x00$.

Fast update: DTM2 image is the NEW image data that you want displaying next moment.

Data	Pixel Color
1	Black
0	White

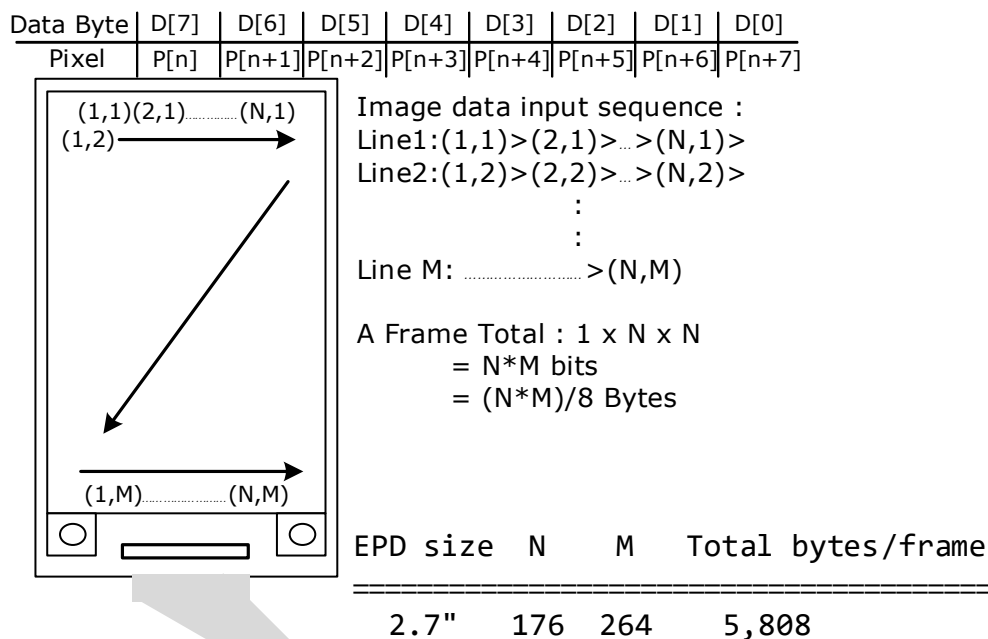
4.1 Image data sending (DTM1, DTM2)

This section describes how to send the DTM1 and DTM2 data and how mapping to real pixel. User needs to send enough image data into COG through both register 0x10(DTM1) and 0x13(DTM2).



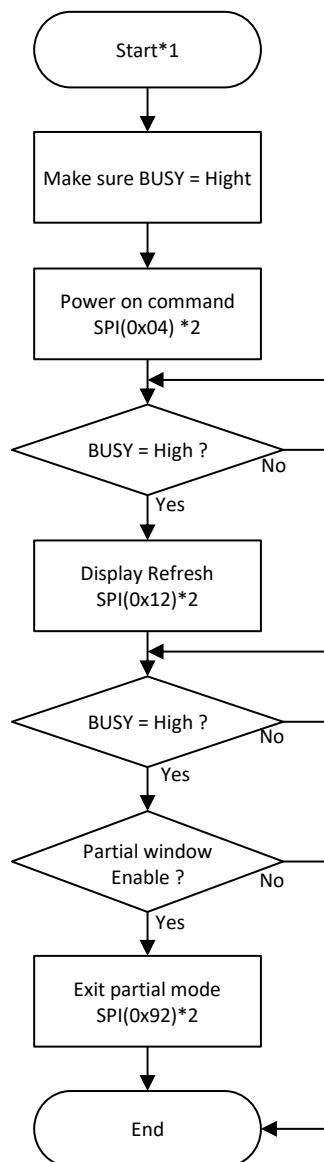
Note 1: $n=(N*M)/8$

The data of image frame, one bit represents 1 pixel. (e.g. the first byte represents the 1st ~ 8th pixels of the first line, the second byte represents the 9th ~ 16th pixels of the first line, and so on).



When enabling "partial window" function, the M and N are variables. They need to be suitable for **PTL**(partial window) settings.

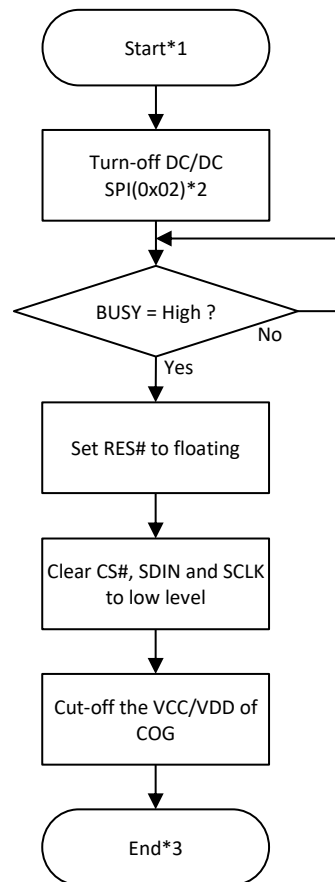
5. Send updating command



Note:

1. Start: Follow the end of the input image sequence
2. This register does not have data, just need send the index

6. Turn-off DC/DC



Note:

1. Start: Follow the end of the send updating command sequence
2. This register does not have data, just need send the index
3. Finished the all of the steps for update the EPD

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Revision History

Version	Date	Page (New)	Section	Description
01	2020/12/14			First issue
02	2020/12/28	3 11~14	1.2 4	1. Redefine the name of operation mode 2. Add the partial window update function
03	2021/5/27	10	3	1. Modify the temperature range

Glossary of Acronyms

EPD	Electrophoretic Display (e-Paper Display)
EPD Panel	EPD
TCon	Timing Controller
FPL	Front Plane Laminate (e-Paper Film)
SPI	Serial Peripheral Interface
COG	Chip on Glass
PDI, PDi	Pervasive Displays Incorporated