Product Specifications

Customer	**STANDARD**
Description	**9.7” TFT EPD Panel**
Model Name	**E2969CS081**
Date	**2019/10/28**
Doc. No.	**1P225-00**
Revision	**01**

Customer Approval	
Date	
The above signature represents that the product specifications, testing regulation, and warranty in the specifications are accepted	

	Design Engineering		
	Approval	**Check**	**Design**
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Table of Contents

List of Figures

List of Tables

Revision History

Version	Date	Page (New)	Section	Description
01	2019/10/28	All	All	Specification first issued

Glossary of Acronyms

COG	Chip on Glass
EPD	Electrophoretic Display (e-Paper Display)
EPD Module	EPD with TCon board
EPD Panel	EPD
FPC	Flexible Printed Circuit
FPL	Front Plane Laminate
IIS	Incoming Inspection Standard
ISTA	International Safe Transit Association
PDI	Pervasive Displays Incorporated
SPI	Serial Peripheral Interface
TCon	Timing Controller
TFT	Thin Film Transistor

1 General Description

1.1 Overview

This is a 9.7” a-Si TFT active matrix Electronic Paper Display (EPD) module. The module has such high resolution (121 dpi) that it is able to easily display fine patterns. Due to its bi-stable nature, the EPD module requires very little power to update and needs no power to maintain an image.

1.2 Features

- a-Si TFT active matrix Electronic Paper Display (EPD)
- Resolution: 672 x 960
- Ultra low power consumption
- Super Wide Viewing Angle - near 180°
- Extra thin & light
- SPI interface
- RoHS compliant
- Wide temperature support

1.3 Applications

- e-POP/Signage
- Electronic bulletins
- Office Automation
- Navigator

1.4 General Specifications

Table 1-1 General Specification

Item	Specification	Unit	Note
Outline Dimension	155.3 (H) x 214.6 (V) x 1.1(T)	mm	(1)
Active Area	141.12 (H) x 201.6 (V)	mm	
Driver Element	a-Si TFT active matrix	-	
FPL	Aurora Mb	-	
Pixel Number	672 x 960	pixel	
Pixel Pitch	0.210 x 0.210 (121 dpi)	mm	
Pixel Arrangement	Vertical stripe	-	
Display Colors	Black/White	-	
Surface Treatment	Anti-Glare	-	
Driver IC	Source (IST7132) / Gate (HX8695)		

Note (1): Not including the FPC.

1.5 Mechanical Specifications

Table 1-2 EPD Mechanical Specification

Item		Min.	Typ.	Max.	Unit	Note
Glass Size	Horizontal(H)	155.1	155.3	155.5	mm	
	Vertical(V)	214.4	214.6	214.8	mm	
	Thickness(T)	1.0	1.1	1.2	mm	(1)
Weight		-	61.5	-	g	

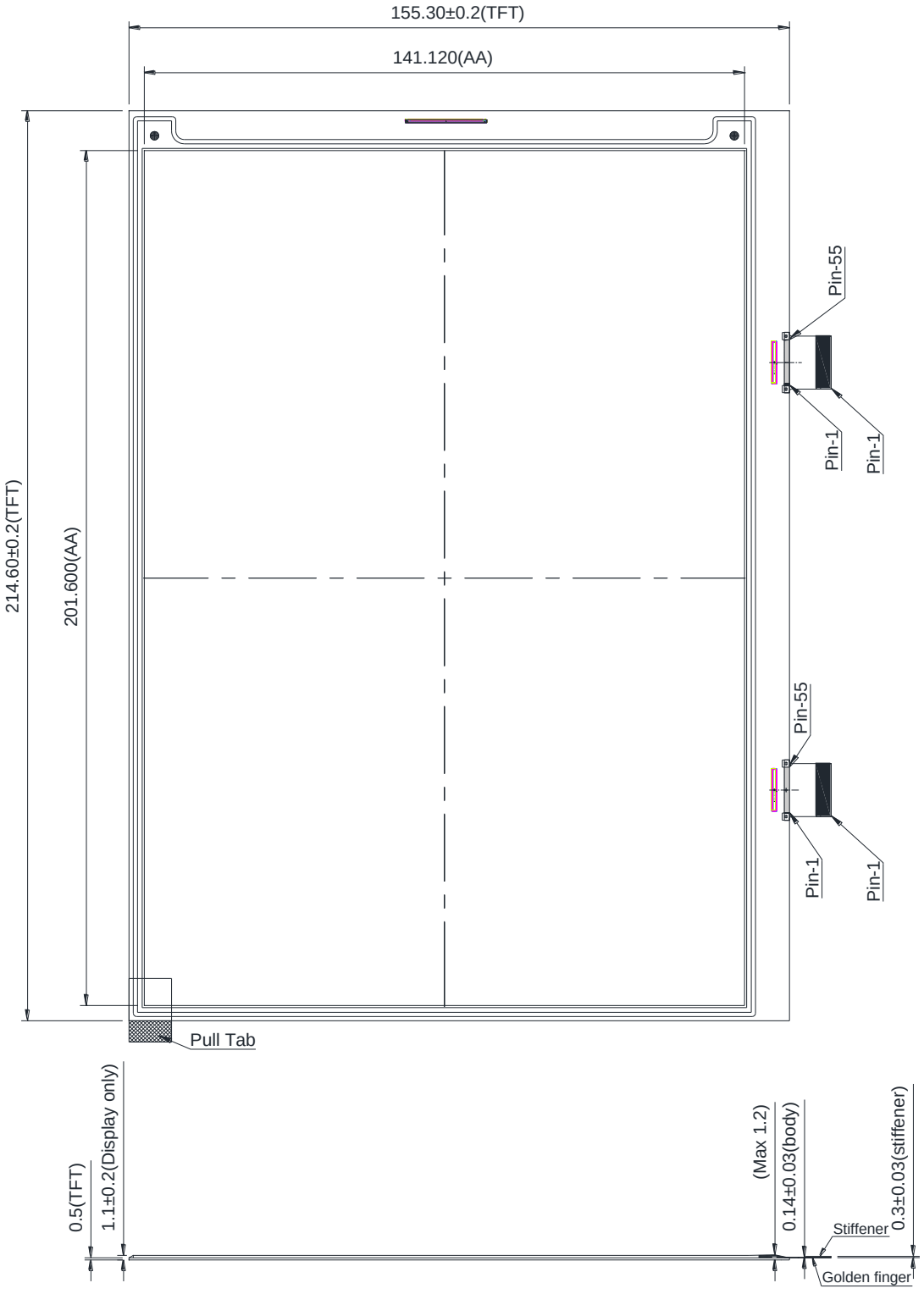
Note (1): Not including the Masking Film.

Table 1-3 FPC Specification

Item	Pin numbers	Pitch (mm)	Connector	Note
Golden Finger	24	0.5	HRS FH34SRJ 24S or Compatible	(1)

Note (1): HRS FH34SRJ 24S is 24-pins connectors. The 24 pins are used to connect FPC pads of EPD.There are two FPCs on EPD panel. Please refer PDI demo kit for detailed connection.

Figure 1-1 EPD Drawing



General tolerance: ±0.3mm

2 Absolute Maximum Ratings

2.1 Absolute Ratings of Environment

Table 2-1 Absolute Ratings of Environment

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1),(3)
Storage Humidity	H_{ST}	40	70	%RH	(1),(3)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1),(2),(4)
Operating Ambient Humidity	H_{OP}	40	70	%RH	(1),(2),(4)
Optimal Storage Temperature	T_{OST}	-10	35	ºC	(1),(3)
Optimal Storage Humidity	H_{OST}	40	60	%RH	(1),(3)

Note (1):

(a) 70 %RH Max. (Ta $\leqq$ 40 ºC), where Ta is ambient temperature.

(b) No condensation and no frost in absolute ratings of Environment.

Note (2): The temperature of panel display surface area should be 0 ºC Min. and 50 ºC Max. Refresh time depends on operation temperature.

Note (3): E Ink Material is Moisture and UV sensitive. The absolute rating operating environments describes the boundary conditions for updating the display while the absolute rating storage environment describe the boundary conditions for a display not updating. While displays are rated to perform according to specification for the warranty period at the absolute specified operating environment, the better the storage condition, the better the E Ink displays will perform. Similar to other moisture and UV sensitive components, we recommend that our displays be stored in temperature and humidity control environments, and whenever possible, under above defined Optimal Storage Condition, away from sunlight, to optimize their performance.

Note (4): The performance of EPD may be degraded under sunlight. Please customer consults PDI if customer wants to use EPD under sunlight.

2.2 Reliability Test Item

Table 2-2 Reliability Test Items

Item	Test Condition	Remark
High Temperature Operation	50 ℃ / 30 %RH for 240h	(1) (2)
Low Temperature Operation	0 ℃ for 240h	(1) (2)
High Temperature/Humidity Operation	40 ℃ / 70 %RH for 240h	(1) (2)
High Temperature Storage	60 ℃ / 40 %RH for 240h	(1)(2)(3)
Low Temperature Storage	-20 ℃ for 240h	(1)(2)(3)
High Temperature/Humidity Storage	60 ℃ / 80 %RH for 240h	(1)(2)(3)
Thermal Cycles (Non-operation)	1 Cycle:-20℃/30min → 60℃/30min, for 100 Cycles	(1)(2)(3)
Package Drop Test	Drop from 97cm. (ISTA) 1 corner, 3 edges, 6 sides. One drop for each.	(1)(2)(3)
Package Random Vibration Test	1.15Grms, 1Hz ~ 200Hz. (ISTA)	(1)(2)(3)

Note (1): No condensation and no frost during test. End of test, function, mechanical, and optical shall be satisfied with product specification and IIS.

Note (2): The test result and judgment are based on PDI's 1bit driving waveform, driving fixture and driving system.

Note (3): Stay white pattern for storage and non-operation test.

2.3 Product Warranty

Warranty conditions have to be negotiated between PDI and individual customers. PDI provides 13 months warranty for all products which are purchased from PDI.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings of Panel

Table 3-1 Absolute Maximum Ratings of Panel

Parameter	Symbol	Value		Unit	Note
		Min	Max		
Digital Power	V_{DDIO}	-0.3	5.0	V	
Analog Power	V_{DD}	-0.3	5.0	V	
Ground	V_{SS}	-		-	Connect V_{SS} to Ground

T_a = 25 ± 2 ºC

3.2 Recommended Operation Conditions of Panel

Table 3-2 Recommended Operation Conditions of Panel

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
VDDIO, VDD operation voltage		V_{DDIO}, V_{DD}	2.3	3.0	3.3	V	
Input Voltage	High	V_{IH}	$0.8V_{DDIO}$	-	V_{DDIO}	V	$V_{DDIO}=V_{DD}$
	Low	V_{IL}	V_{SS}	-	$0.2V_{DDIO}$	V	
Output Voltage	High	V_{OH}	$0.8V_{DDIO}$	-	V_{DDIO}	V	$V_{DDIO}=V_{DD}=2.4V$ $I_{OUT}=1mA$
	Low	V_{OL}	V_{SS}	-	$0.2V_{DDIO}$	V	$V_{DDIO}=V_{DD}=2.4V$ $I_{OUT}=-1mA$,
Input Current (standard price / bit_checkered)		I_{CC}	-	14.3 / 26.4	-	mA	(1), (2), (3) FPl lot: VEU025 Q'ty: 5pcs
Peak Current (standard price / bit_checkered)		I_{PEAK}		55.9/ 104.6		mA	
Power Consumption (standard price / bit_checkered)		-		358.9/ 665.0		mAs	

T_a = 25 ± 2 ºC

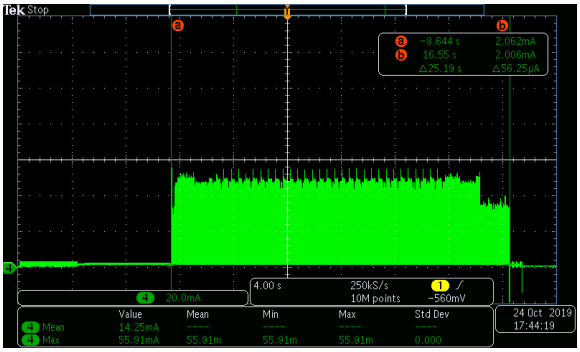
Note (1):

Figure 3-1 Test Pattern of Panel

These currents are tested with PDI test jig.

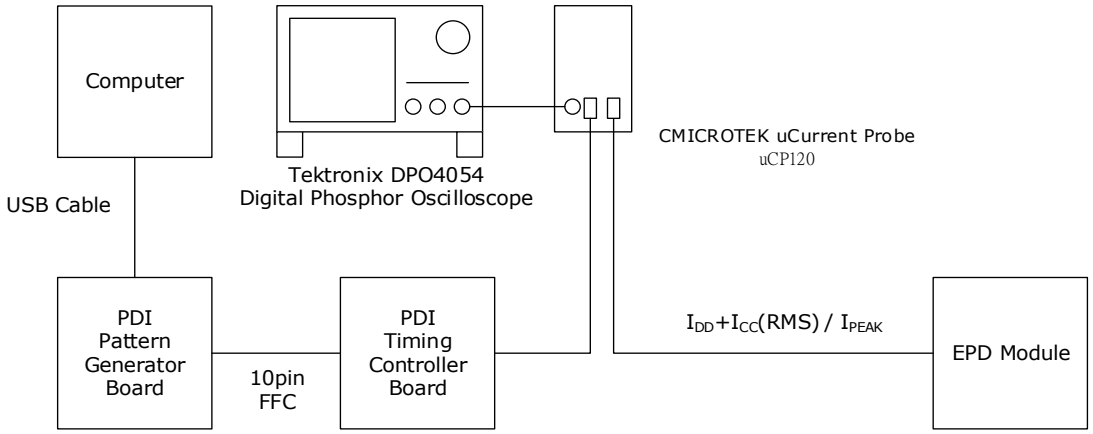
Note (2): $V_{DDIO}=V_{DD}=3.0V$

Figure 3-2 Image Update Current Profile



Note (3):

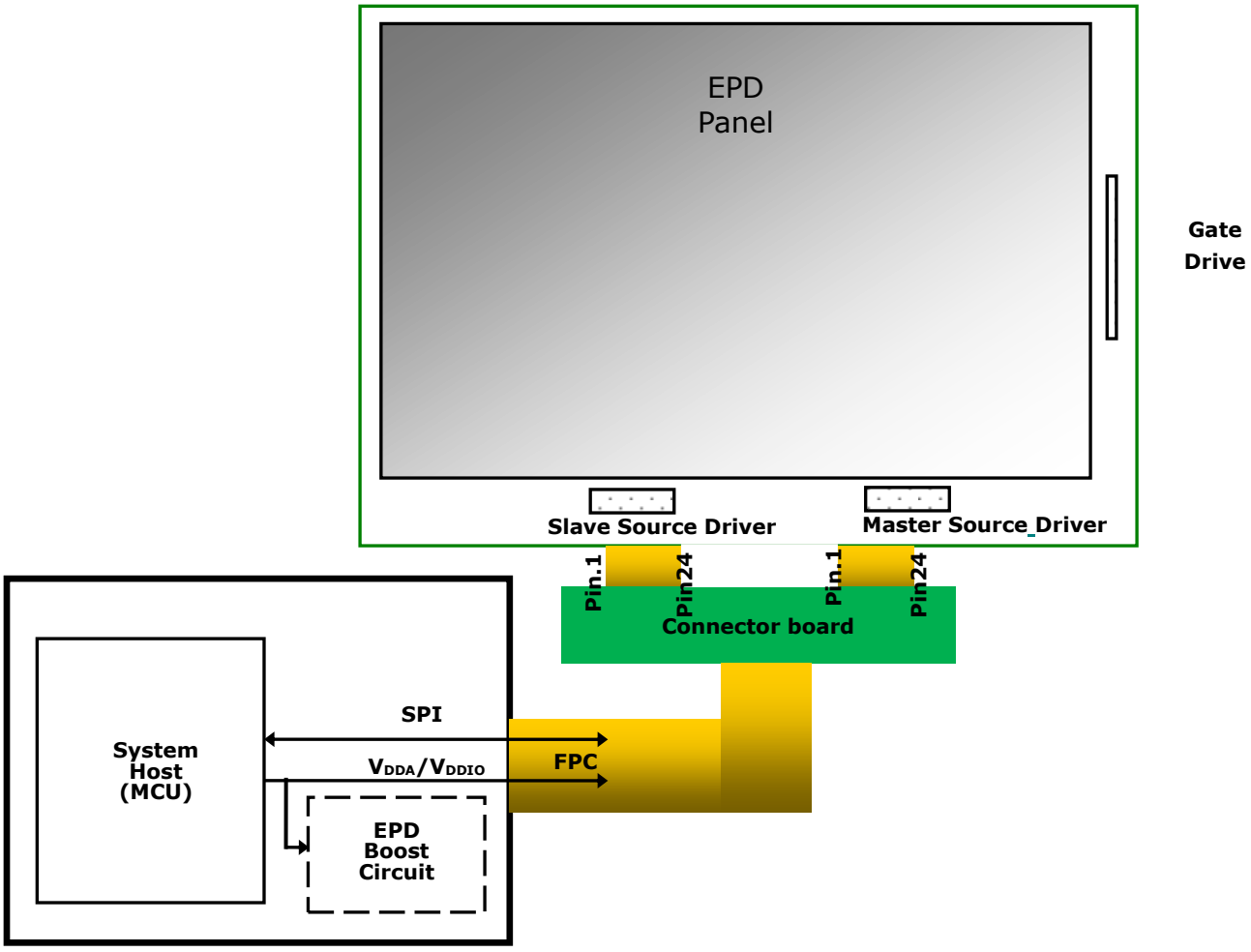
Figure 3-3 Current Measurement



*Set oscilloscope filter to 250MHz and record length to 10M points.

4 Application Circuit Block Diagram

Figure 4-1 Application Circuit Block Diagram



5 Terminal Pin Assignment & Reference Circuit

5.1 Terminal Pin Assignment

Table 5-1 Terminal Pin Assignment (Master FPC)

No.	Signal	Type	Connected to	Function
1	FSYNC	I/O	Slave FSYNC	Cascade line frame sync
2	NGDRV	O	Power MOSFET Driver control	This pin is the N-Channel MOSFET Gate Drive Control.
3	RESE	I	Booster Control Input	This pin is the Current Sense Input for the Control Loop.
4	INTERNAL_VPP	P	VPP PIN & Slave FPC	MTP power internal
5	NC	C	-	NC
6	LNSYNC	I/O	Slave LNSYNC	Cascade line sync
7	CLK	I/O	Slave CLK	Cascade clock
8	BS	I	VSS	This pin is setting panel interface.
9	M_BUSY	O	Device Busy Signal	This pin is Busy state output pin of the master chip. When Busy is Low, the operation of the chip should not be interrupted, and Command should not be sent.
10	RESETB	I	System Reset	This pin is reset signal input. Active Low.
11	A0	I	VDDIO or VSS	This pin is Data/Command control.
12	M_CSB	I	VDDIO or VSS	This pin is the Master chip select.
13	SCL	I	Data Bus	Serial communication clock input.
14	SDA	I	Data Bus	Serial communication data input/output.
15	VDDIO	P	Power Supply	Power for interface logic pins & I/O. It should be connected with VDDIO.
16	VDD	P	Power Supply	Power Supply for the chip.
17	VSS	P	Ground	Ground
18	VDDL	C	Capacitor	Internal regulator output A capacitor should be connected between VDDL and VSS.

No.	Signal	Type	Connected to	Function
19	VPP	P	INTERNAL_VP& Slave VPP	MTP power
20	VDH	C	Capacitor	This pin is the Positive Source driving voltage. A stabilizing capacitor should be connected between VDH and VSS.
21	VGH	C	Capacitor	This pin is the Positive Gate driving voltage A stabilizing capacitor should be connected between VGH and VSS.
22	VDL	C	Capacitor	This pin is the Negative Source driving voltage. A stabilizing capacitor should be connected between VDL and VSS.
23	VGL	C	Capacitor	This pin is the Negative Gate driving voltage. A stabilizing capacitor should be connected between VGL and VSS.
24	VCOM	C	Capacitor	This pin is the VCOM driving voltage A stabilizing capacitor should be connected between VCOM and VSS.

Table 5-2 Terminal Pin Assignment (Slave FPC)

No.	Signal	Type	Connected to	Function
1	FSYNC	I/O	Master FSYNC	Cascade line frame sync
2	NC	-	-	Not connected
3	NC	-	-	Not connected
4	NC	-	-	Not connected
5	NC	-	-	Not connected
6	LNSYNC	I/O	Master LNSYNC	Cascade line sync
7	CLK	I/O	Master CLK	Cascade clock
8	BS	I	VSS	This pin is setting panel interface.
9	S_BUSY	O	Device Busy Signal	This pin is Busy state output pin of the slave chip. When Busy is Low, the operation of the chip should not be interrupted, and Command should not be sent.
10	RESETB	I	System Reset	This pin is reset signal input. Active Low.

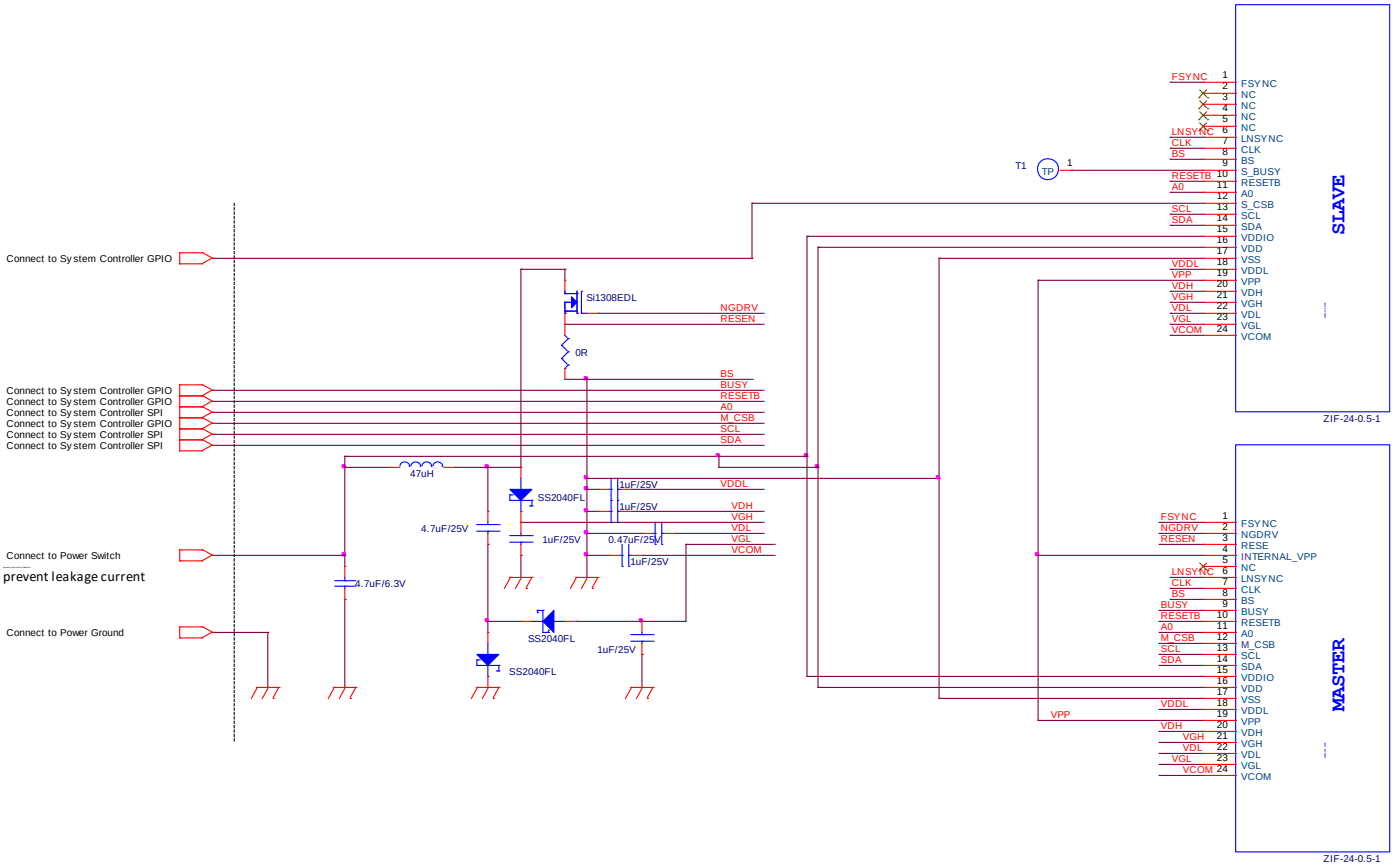
No.	Signal	Type	Connected to	Function
11	A0	I	VDDIO or VSS	This pin is Data/Command control.
12	S_CSB	I	VDDIO or VSS	This pin is the Slave chip select.
13	SCL	I	Data Bus	Serial communication clock input.
14	SDA	I	Data Bus	Serial communication data input/output.
15	VDDIO	P	Power Supply	Power for interface logic pins & I/O. It should be connected with VDDIO.
16	VDD	P	Power Supply	Power Supply for the chip.
17	VSS	P	Ground	Ground
18	VDDL	C	Capacitor	Internal regulator output A capacitor should be connected between VDDL and VSS.
19	VPP	P	Master VPP	MTP power
20	VDH	C	Capacitor	This pin is the Positive Source driving voltage. A stabilizing capacitor should be connected between VDH and VSS.
21	VGH	C	Capacitor	This pin is the Positive Gate driving voltage A stabilizing capacitor should be connected between VGH and VSS.
22	VDL	C	Capacitor	This pin is the Negative Source driving voltage. A stabilizing capacitor should be connected between VDL and VSS.
23	VGL	C	Capacitor	This pin is the Negative Gate driving voltage. A stabilizing capacitor should be connected between VGL and VSS.
24	VCOM	C	Capacitor	This pin is the VCOM driving voltage A stabilizing capacitor should be connected between VCOM and VSS.

Note:

Type: I: Input
O: Output
C: Capacitor
P: Power

5.2 Reference Circuit

Figure 5-1 EPD Reference Circuit



Type	Part	Quantity	Vendor	Note
Inductor	47uH 0.3A ETPRH3D16B-470M	1pc	ARLITECH	
Transistor	Si1308EDL SOT-23 N-Channel	1pc	Vishay	(1)
Diode	SS2040FL SOD-123FL	3pcs	PANJIT	(2)
Capacitors	4.7uF/25V	2pc	-	
Capacitors	1uF/25V	5pcs	-	
Capacitors	0.47uF/25V	1pcs	-	
Resistors	0R ohm/1%	1pc	-	

Note:

(1) Si1308EDL is a N-Channel Power MOSFET. The specification of selection criteria are RDS<185 mohm (the lower the better),VGS<2.5V@Id=0.5A.

(2) SS2040FL is a Schottky diode needs the Vf as lower as possible, 0.2 to 0.4V and the repetitive peak reverse voltage > 25V.

6 Optical Characteristics

6.1 Measurement Conditions

Table 6-1 Optical Measurement Conditions

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	ºC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{DDIO} & V_{DD}	3.0	V

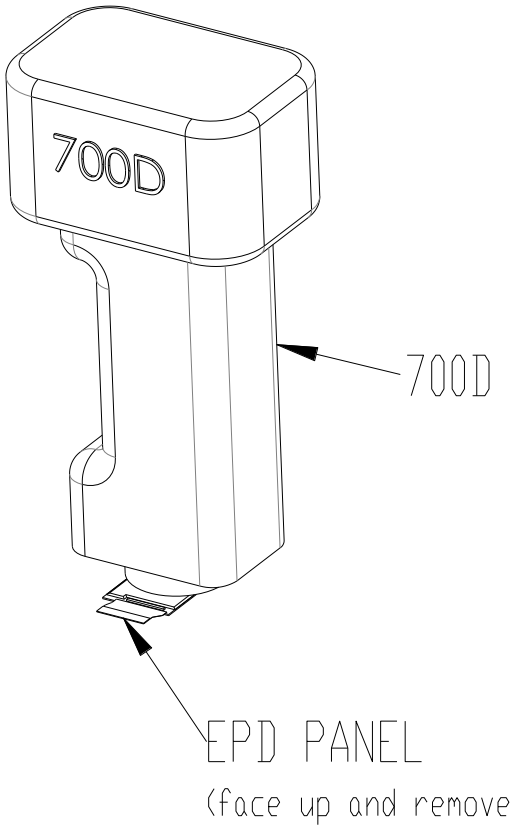
6.2 Optical Specifications

Table 6-2 Optical Measurement with D65 light source

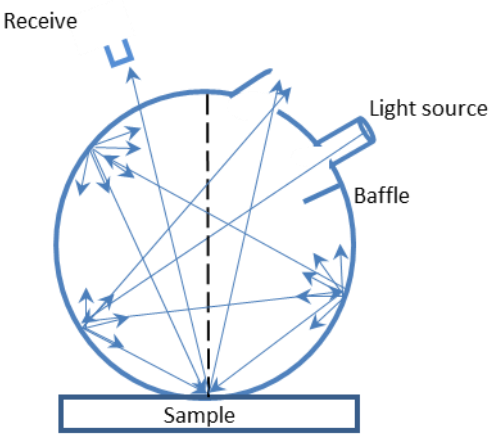
Item	Symbol	Rating			Unit	Note
		Min.	Typ.	Max.		
Contrast ratio	CR	-	18:1	-	-	θx=θy=0 (1),(2),(4),(5)
Refresh time	Tr	-	25.2	-	sec	(1),(3),(5)
White state	L*	-	72.70	-	-	θx=θy=0 (1),(2),(5)
	a*	-	-3.12	-		
	b*	-	2.88	-		
Reflectance	R%	-	44.7	-	%	(1),(2),(5)

Note (1): Panel is driven by PDI waveform without masking film and optical measurement by CM-700D with D65 light source and SCE mode.

Figure 6-1 Optical Measurement

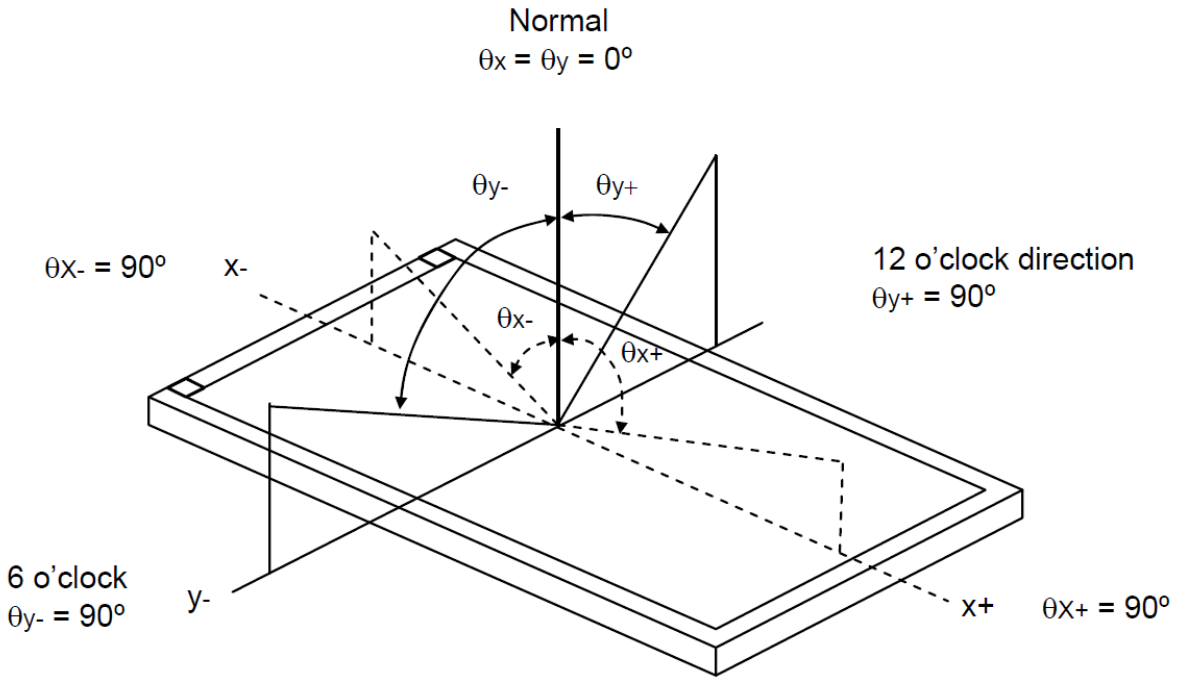


SCE mode



Note (2): Definition of Viewing Angle (θx, θy):

Figure 6-2 Definition of Viewing Angle to Measure Contrast Ratio



Note (3): Refresh time is the time that e-paper particles move not including the power on and off time. The refresh time is measured at 25ºC.The refresh time and contrast ratio varies due to different films, display performance requirements, and ambient temperatures.

Note (4): Contrast ratio (C.R.): The Contrast ratio is calculated by the following expression. C.R. = (R% White) / (R% Black).

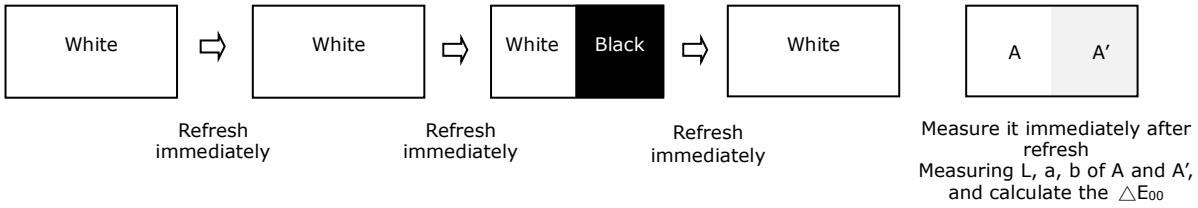
Note (5): Optical data is measured at 60 seconds after refresh with PDI's global update procedure.

6.3 Ghosting

Below are two test methods to verify if ghosting is within an acceptable range. Test 1 and Test 2 use measured data to calculate color different, $\triangle E_{00}$ (CIEDE 2000).

The condition of measurement is to follow " Table 6-1 Optical Measurement Conditions".

- Test 1: White to Black Ghosting



- Test 2: Black to White Ghosting

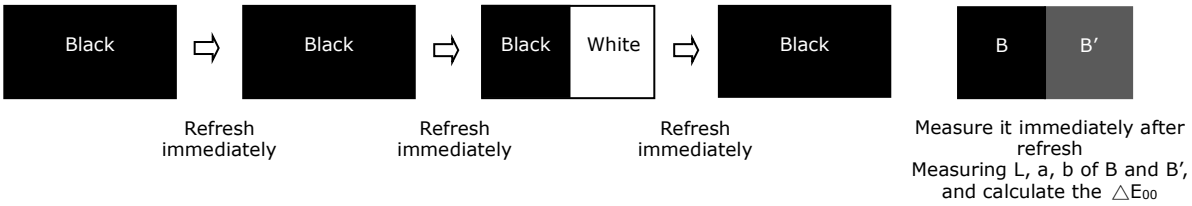


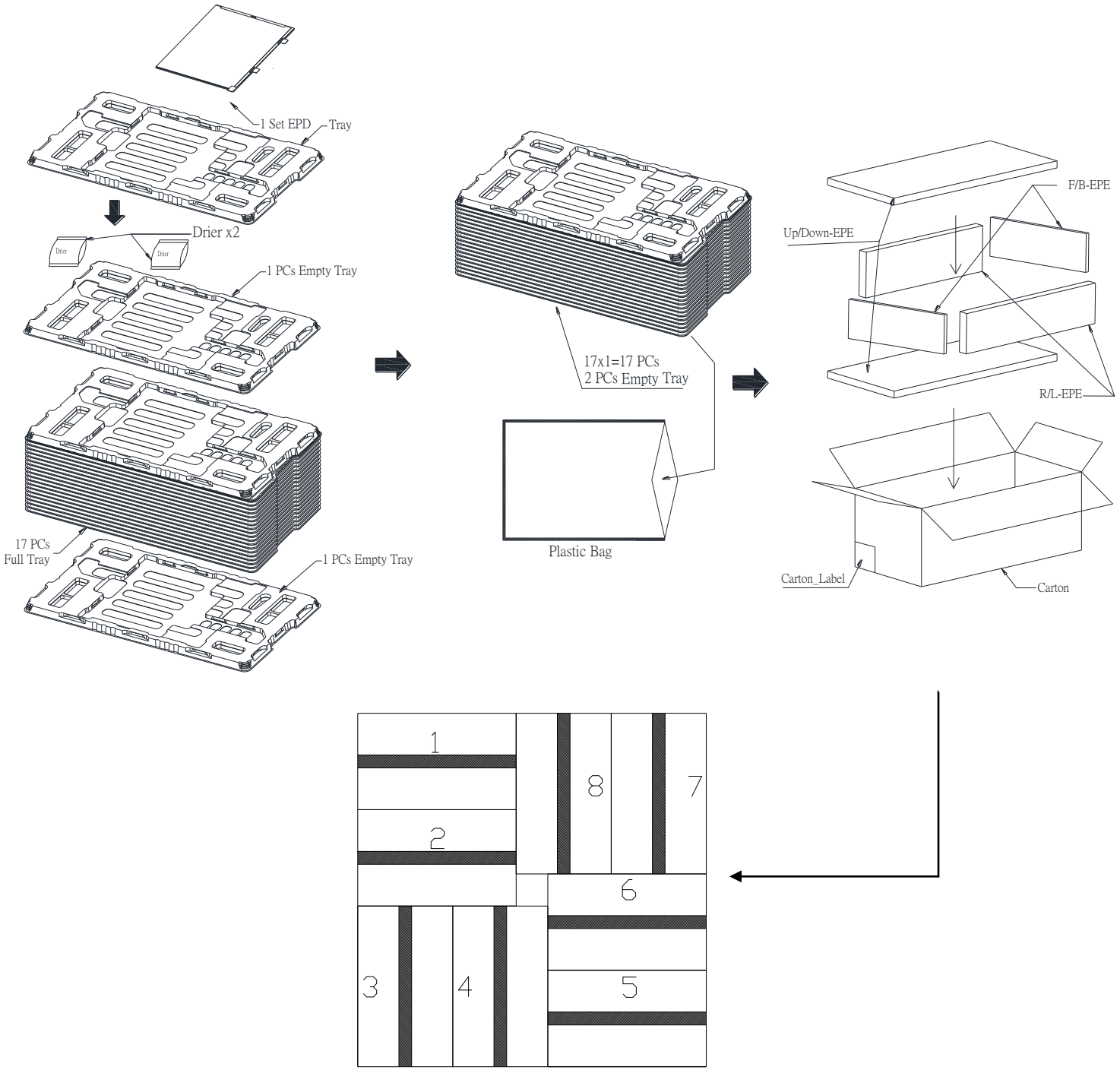
Table 6-3 Measurement of Ghosting

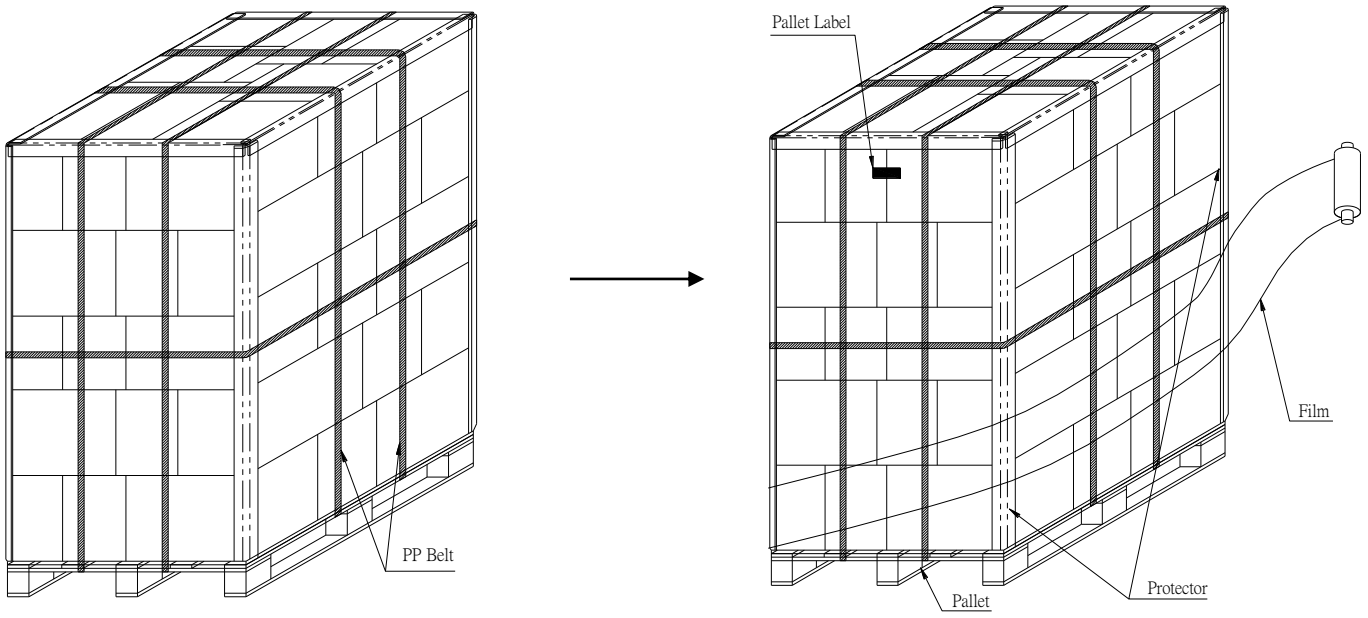
Item	Rating		
	Min.	Typ.	Max.
Test 1 $\triangle E_{00}$	-	-	2
Test 2 $\triangle E_{00}$	-	-	2

Note: Panel is driven by PDI waveform without masking film and optical is measured by CM-700D with D65 light source and SCE mode.

7 Packing

Figure 7-1 Packing Diagram

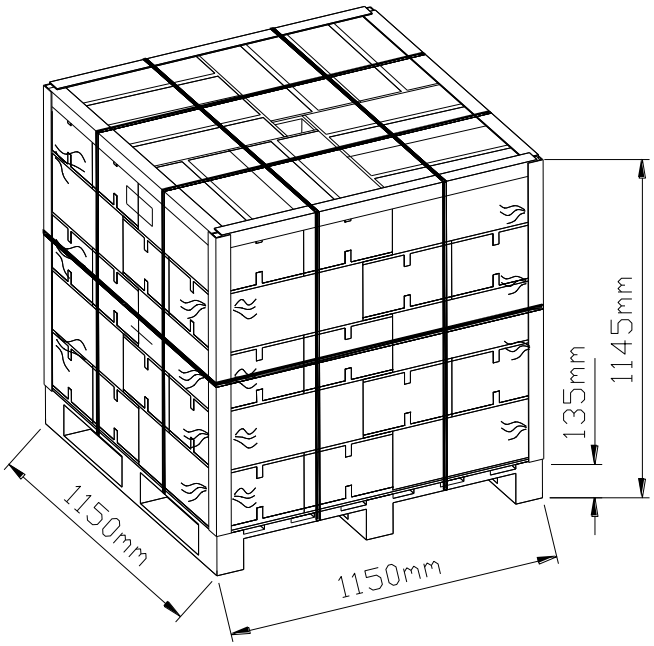




17(pcs)x40(BOX)=680pcs

	9.7″ EPD BOX
N.W.:	1.05 Kg
G.W.:	4.53 Kg

Sea / Land / Air Transportation



8 Precautions

(1) The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel during assembly. Please put on gloves to handle EPD to avoid slash.

(2) It is recommended to assemble or install EPD panels in a clean working area. Dust and oil may cause electrical shorts or degrade / scratch / den the protection sheet film.

(3) Do not apply pressure to the EPD panel in order to prevent damaging it.

(4) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(5) Please support the bezel with your finger while connecting the interface cable such as the FPC.

(6) Do not stack the EPD panels / Modules.

(7) Do not press the FPC on the glass edge or Pull FPC up / down to 90°.

(8) Do not touch the FPC lead connector.

(9) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(10) Wear a Wrist Strap (Grounding connect) when handling and during assembly. Semiconductor devices are included in the EPD Panel / Module and they should be handled with care to prevent any electrostatic discharge (ESD). (An Ion Fan may be needed in assembly operation to reduce ESD risk.)

(11) Keep the EPD Panel / Module in the specified environment and original packing boxes when storage in order to avoid scratching and keep original performance.

(12) Do not disassemble or reassemble the EPD panel.

(13) Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating. This behavior would make dent or scratch on protection sheet.

(14) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(15) It's low temperature operation product. Please be mindful the temperature different to make frost or dew on the surface of EPD panel. Moisture may penetrate into the EPD panel because of frost or dew on surface of EPD panel, and makes EPD panel damage.

(16) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended that customer refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue.

(17) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

(18) The label ink used for marking the Panel ID number is erased easily by solvent. Please avoid using solvent to clean the EPD panel. It would be concerned for RMA.

(19) The EPD / Module is vacuum packed with white image for shipment and storage.

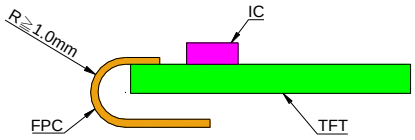
(20) Before approved by PDI and customer, products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.

(21) PDI makes every attempt to ensure that its products are of high quality and reliability. However, contact PDI sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.

(22) Design your application so that the product is used within the ranges guaranteed by PDI particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. PDI bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail safes, so that the equipment incorporating PDI product does not cause bodily injury, fire or other consequential damage due to operation of the PDI product.

(23) This product is not designed to be radiation resistant.

(24) Please keep R≧1.0mm when bend for assembly.



9 Definition of Labels

Figure 9-1 Model Labels

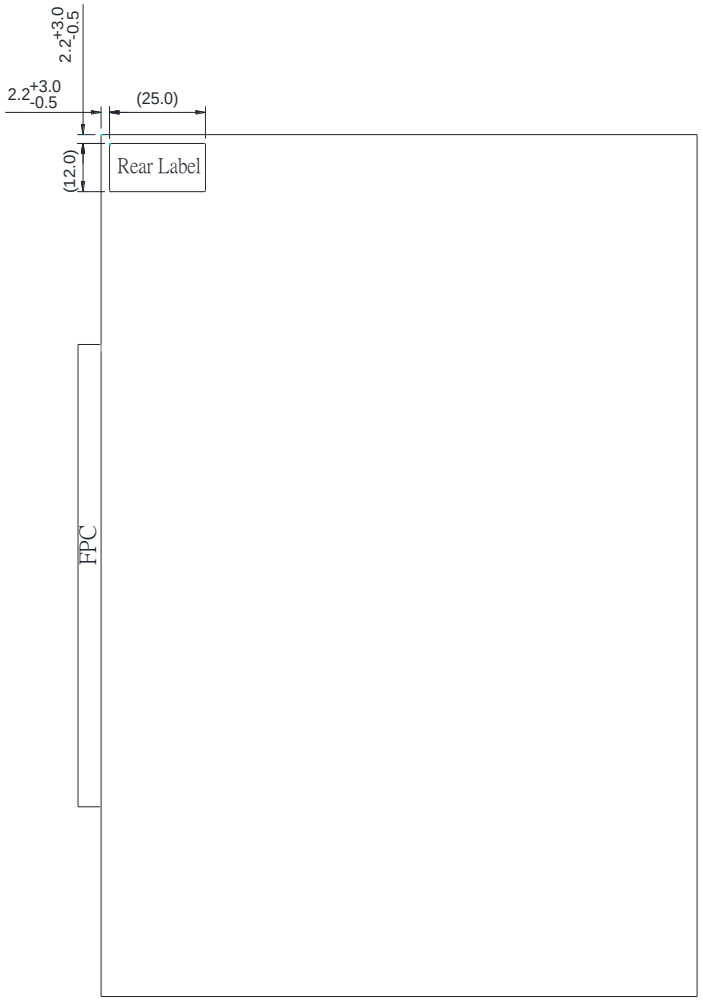


Figure 9-2 Definition of Model Labels

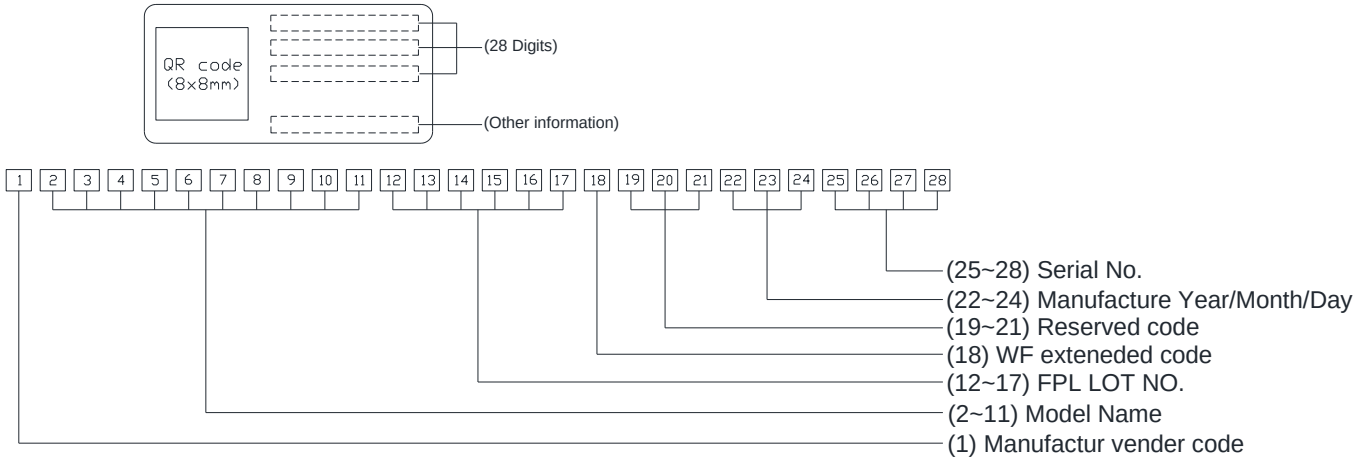


Figure 9-3 Carton Label

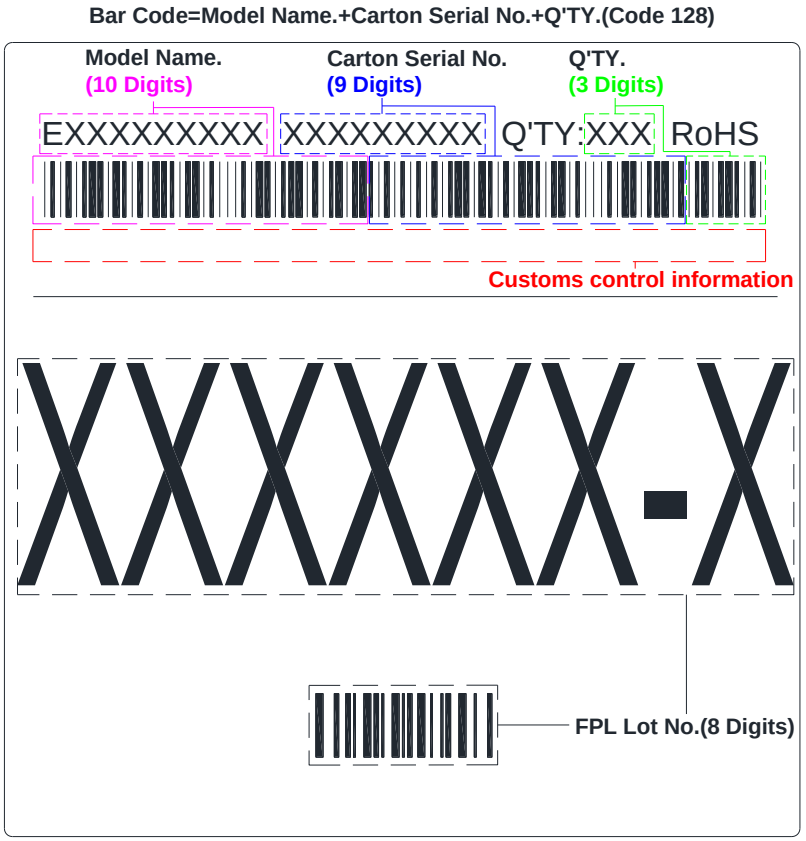


Figure 9-4 Pallet Label