

Application Note

For

5.8" Fast update EPD (E2581PS0B1)

| | |
|--------------------|--|
| Description | Interface for the 5.8" Fast update EPD (E2581PS0B1) |
| Date | 2023/2/6 |
| Doc. No. | |
| Revision | 02 |

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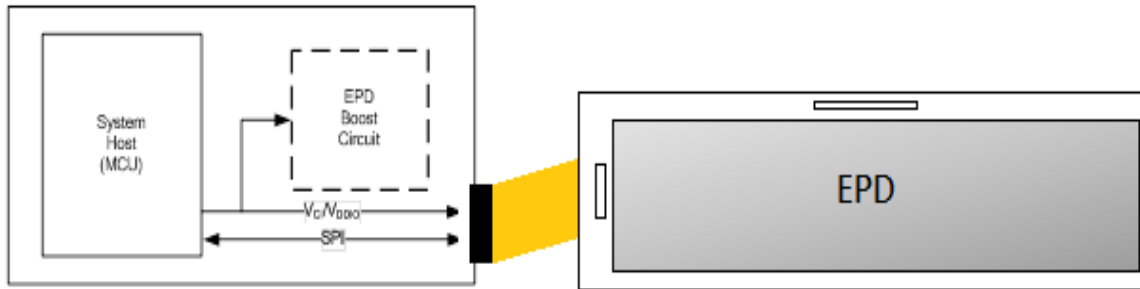
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1 General Description

1.1 Overview

The document introduces how to drive the 5.8" Fast update EPD(E2581PS0B1). The EPD has embedded the Tcon function. The major control interface of the driver is SPI. The host sends both the setting commands and the display image to driver through the SPI bus.



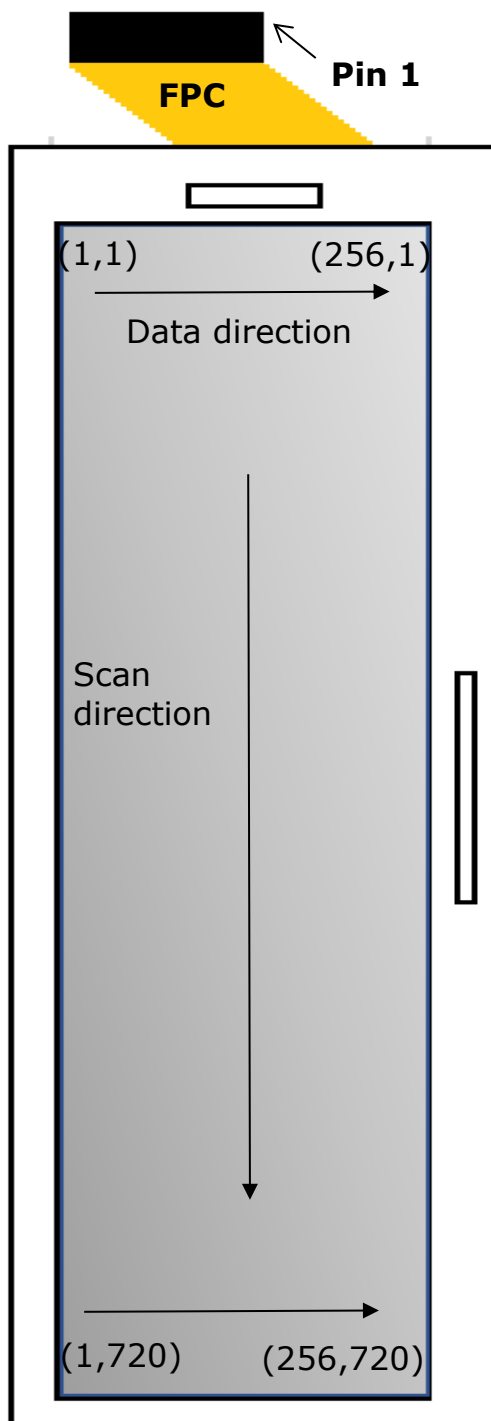
1.2 Definition of operation mode

The section will define and clarify update modes.

Normal update: it will perform the complete waveform for image update. The process will go through the inverse, shaking and imaging phases. The mode will take more time, but it will bring better image performance.

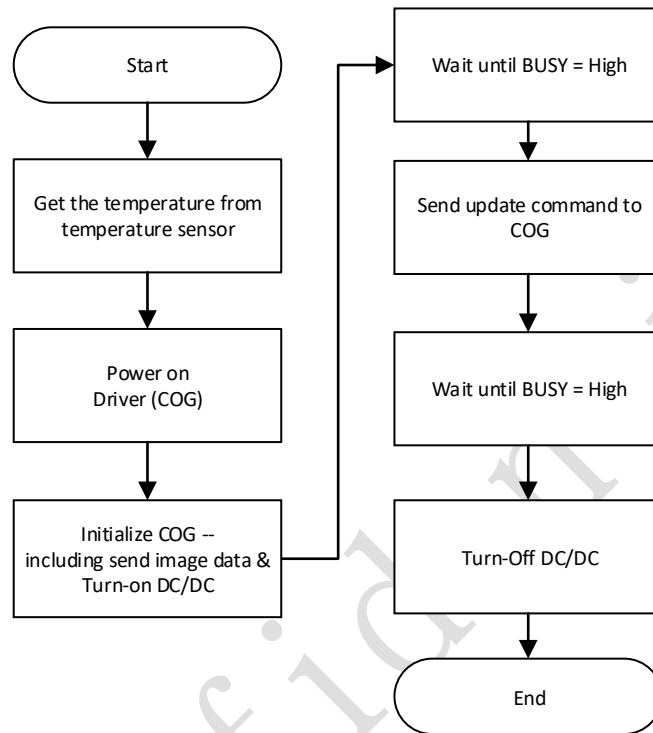
Fast update: the short waveform will be executed. COG compares the pixel data of the current image and the new image pixel by pixel, and then only drives the transition pixels. The mode can quickly complete the image update.

1.3 Panel drawing



1.4 EPD Driving Flow Chart

The flowchart below provides an overview of the necessary actions to update the EPD. The steps below refer to the detailed descriptions in the respective sections.



1.5 SPI Timing Format

SPI commands are used to communicate between the MCU and the COG Driver. The SPI format used differs from the standard in that two-way communications are not used. When setting up the SPI timing, PDI recommends verify both the SPI command format and SPI command timing in this section.

The maximum clock speed of the display is **5MHz(write) , 1.66MHz(read)**.

- Below is a description of the SPI Format:

SPI(0xI, 0xD₁, 0xD₂, ..., 0xD_n)

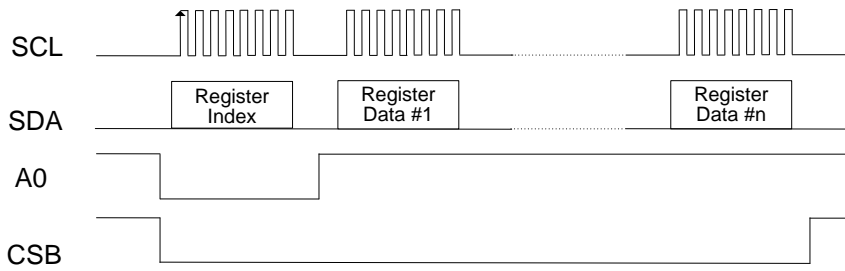
Where:

I is the Register Index and the length is 1 byte

D_{1~n} is the Register Data. The Register Data length is variously.

- When SPI sends the Index, the A0 has to pull LOW. When sends the data, the A0 has to pull HIGH. The next page is the detail flow chart.

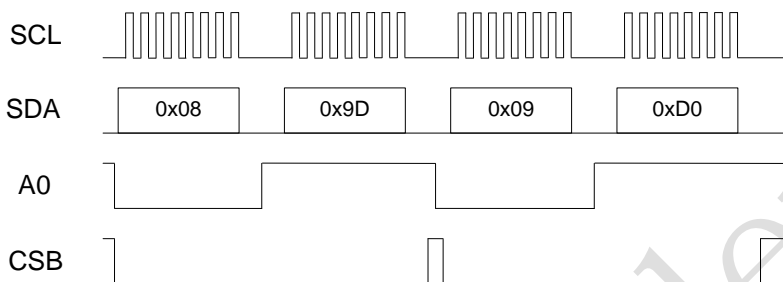
- SPI command signals and flowchart:



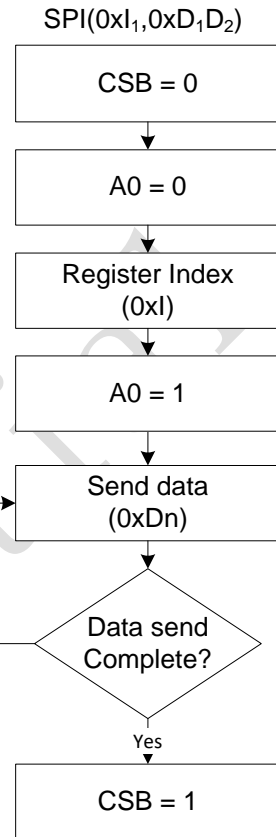
For example:

To send two SPI commands:

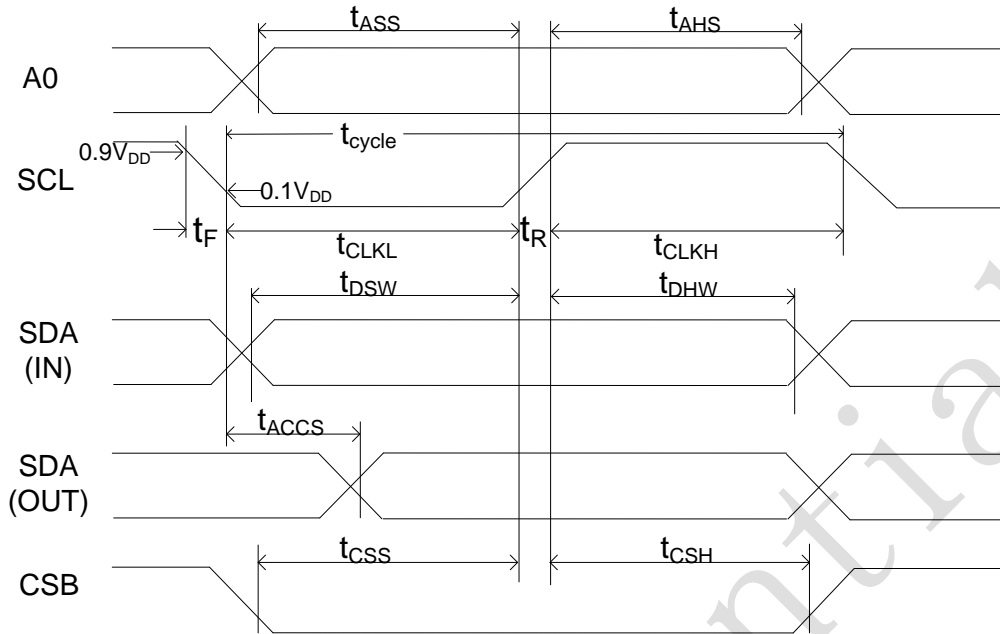
SPI((0x08,0x9D) and SPI(0x09, 0xD0)



If register data is larger than two bytes, you must input data continuously without setting Register Index again.



- SPI command timing



SPI DATA-IN

| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
|------------------------|-------------|------|------|------|------|--------|
| Clock Cycle Time | t_{cycle} | 200 | - | - | ns | |
| Chip Select Setup Time | t_{CSS} | 90 | - | - | ns | |
| Chip Select Hold Time | t_{CSH} | 90 | - | - | ns | |
| Write Data Setup Time | t_{DSW} | 90 | - | - | ns | |
| Write Data Hold Time | t_{DHW} | 90 | - | - | ns | |
| A0 Setup Time | t_{ASS} | 90 | - | - | ns | |
| A0 Hold Time | t_{AHS} | 90 | - | - | ns | |
| Clock Low Time | t_{CLKL} | 90 | - | - | ns | |
| Clock High Time | t_{CLKH} | 90 | - | - | ns | |
| Rise Time [10% ~ 90%] | t_R | - | - | 15 | ns | |
| Fall Time [90% ~ 10%] | t_F | - | - | 15 | ns | |

SPI DATA-OUT (read)

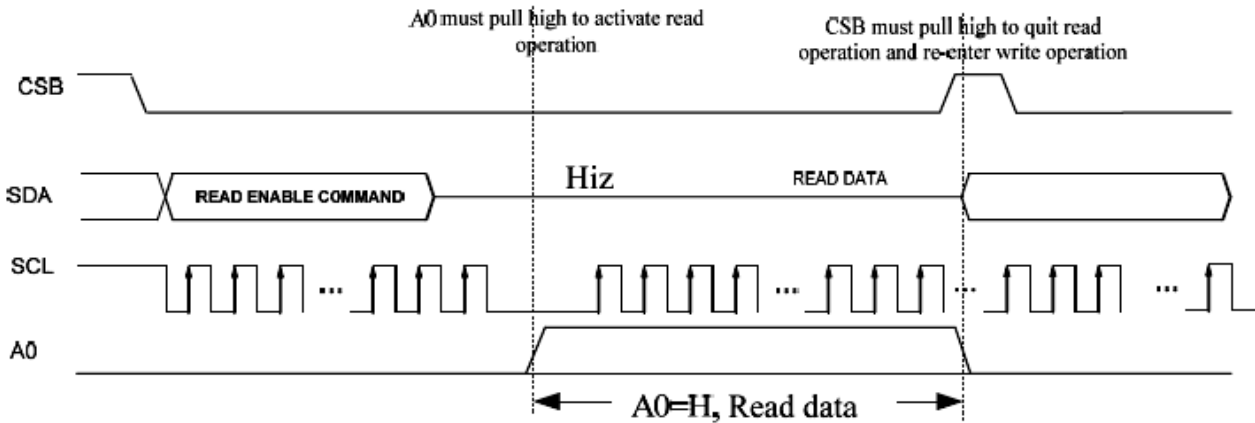
| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
|------------------------|-------------|------|------|------|------|--------|
| Clock Cycle Time | t_{cycle} | 600 | - | - | ns | |
| Chip Select Setup Time | t_{CSS} | 400 | - | - | ns | |
| Chip Select Hold Time | t_{CSH} | 150 | - | - | ns | |
| Read access time | t_{ACCS} | - | - | 200 | ns | |
| A0 Setup Time | t_{ASS} | 90 | - | - | ns | |
| A0 Hold Time | t_{AHS} | 90 | - | - | ns | |
| Clock Low Time | t_{CLKL} | 400 | - | - | ns | |
| Clock High Time | t_{CLKH} | 150 | - | - | ns | |
| Rise Time [10% ~ 90%] | t_R | - | - | 15 | ns | |
| Fall Time [90% ~ 10%] | t_F | - | - | 15 | ns | |

VCC = 2.3 to 3.6V

Temp = 0 to +50°C

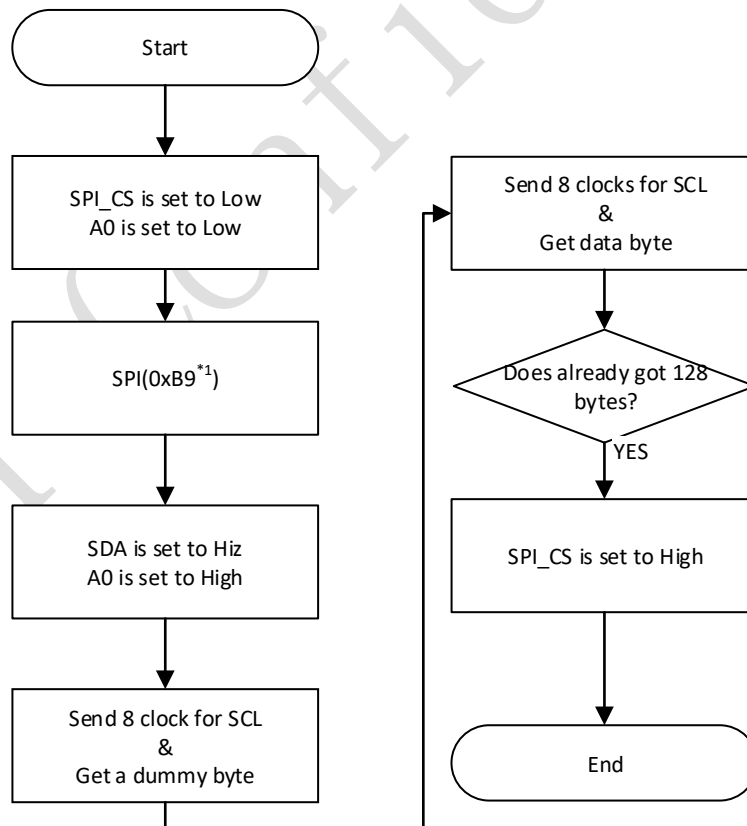
1.6 Read OTP data

The 128-bytes section of OTP have saved the user-defined data that includes the information of the display and soft-start parameters. The section will introduce how to read out the data through the SPI.



- Note: 1. After read enable command is set, SDA must set Hiz, and A0 set high to active read operation
 2. When read operation is done, CSB must set high once to quit read operation.

Read operation of 4-Line SPI



1.7 User-defined data

User's firmware needs to read out the user-defined data with 0xB9 command, and to initialize the COG with the parameters.

| ADDR | CONTENT | BYTE |
|-------------------|--|---------|
| 0x00 | Reserved | 1 Byte |
| 0x01 | COG Type | 1 Byte |
| 0x02 | Vender | 1 Byte |
| 0x03 | Waveform Rev | 1 Byte |
| 0x04 0x09 | FPL lot name (6 bytes of ACSII characters) | 6 Byte |
| 0x0A | Color | 1 Byte |
| 0x0B | TCON | 1 Byte |
| 0x0C | DRFW0 | 1 Byte |
| 0x0D | DRFW1 | 1 Byte |
| 0x0E | DRFW2 | 1 Byte |
| 0x0F | DRFW3 | 1 Byte |
| 0x10 | DCTL | 1 Byte |
| 0x11 | VCOM | 1 Byte |
| 0x12 | RAM R/W Start 0 | 1 Byte |
| 0x13 | RAM R/W Start 1 | 1 Byte |
| 0x14 | RAM R/W Start 2 | 1 Byte |
| 0x15 | DUW 0 | 1 Byte |
| 0x16 | DUW 1 | 1 Byte |
| 0x17 | DUW 2 | 1 Byte |
| 0x18 | DUW 3 | 1 Byte |
| 0x19 | DUW 4 | 1 Byte |
| 0x1A | DUW 5 | 1 Byte |
| 0x1B | STV_DIR | 1 Byte |
| 0x1C | MS_SYNC | 1 Byte |
| 0x1D | BVSS | 1 Byte |
| 0x1E | Flags | 1 Byte |
| 0x1F 0x27 | Reserved | 9 Byte |
| 0x28 0x2F | Stage 1 of the booster boot sequence | 8 Byte |
| 0x30 0x37 | Stage 2 of the booster boot sequence | 8 Byte |
| 0x38 0x3F | Stage 3 of the booster boot sequence | 8 Byte |
| 0x40 0x47 | Stage 4 of the booster boot sequence | 8 Byte |
| 0x48 0x7F | Reserved | 56 Byte |

COG Type(0x01): 0x63 -> single-chip

Vendor(0x02): 0x01 -> PDI

Waveform Rev.(0x03): revision of the waveform

FPL lot name(0x04~0x09): Display FPL-LOT number with 6-character ASCII

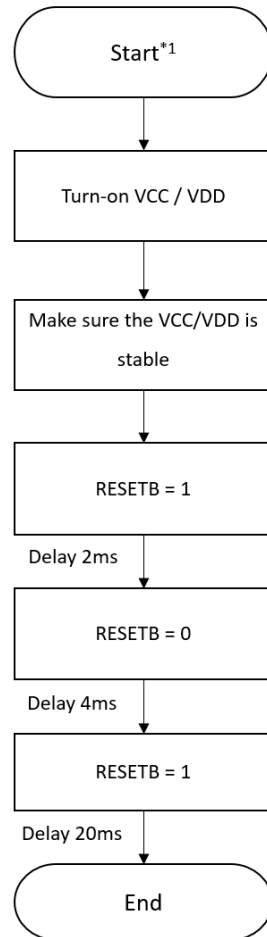
Color(0x0A): 0x00 -> Black/White

Flags(0x1E): 0xFE -> Fast update is supported.

Others(0x0B ~ 0x47): the area data will be used on initial process. They will be mentioned on following sections.

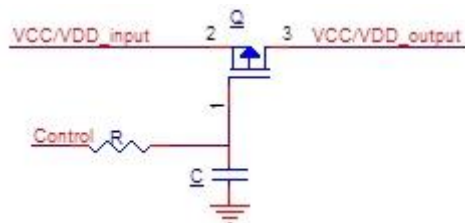
2 Power on COG driver

This flowchart describes power sequence for driver chip.



Note:

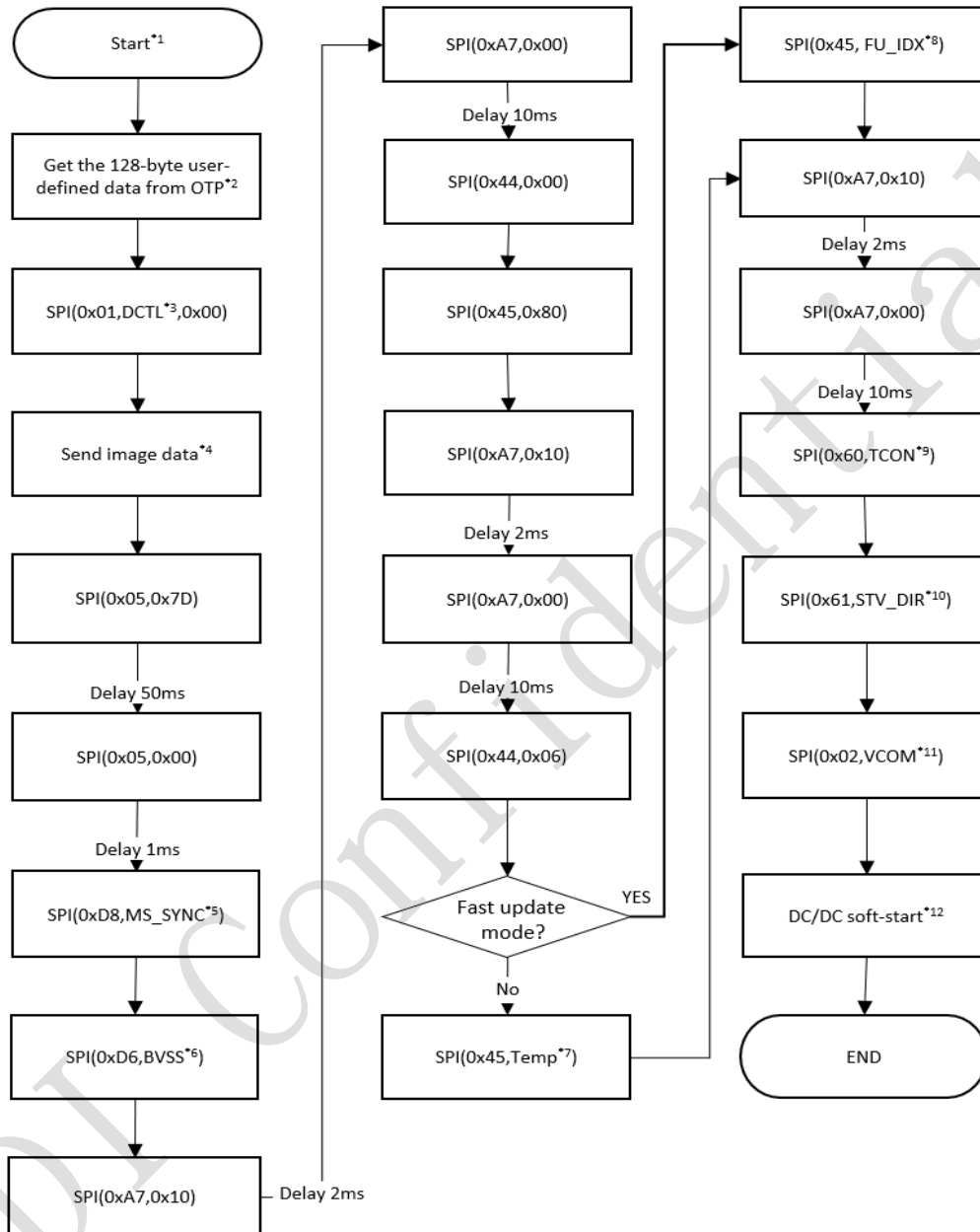
1. **Start:** is the initial state. VCC/VDD, RESETB, CSB, SDA, SCL must be kept at 0v. In order to the inrush current will cause other issue. It is recommended to add soft-start when VCC/VDD is turned on.



VCC/VDD soft-start

3 Initialize COG Driver

3.1 Initial flow chart



Note:

1. **Start:** Follow the end of the power on sequence
2. Please refer to section 1.7 to get the 128-bytes of the user-defined.
3. **DCTL** is read from 0x10 of OTP memory (section1.7)
4. Please refer to section 3.2
5. **MS_SYNC** is read from 0x1C of OTP memory(section1.7)
6. **BVSS** is read from 0x1D of OTP memory(section1.7)
7. **Temp** is an index of the **Normal Update**. The acceptable range of temperature is 0°C ~ 50°C and 1°C per step. **Temp** = temperature + 0x28.

Such as,

$$0^{\circ}\text{C} = 0x28,$$

$$25^{\circ}\text{C} = 0x41,$$

$$50^{\circ}\text{C} = 0x5a$$

If temperature higher than 50°C, just set to 0x5a.(Normal Update)

If temperature lower than 0°C, just set to 0x28.(Normal Update)

8. **FU_IDX** is an index of the **Fast Update**. $\text{FU_IDX} = (\text{temperature} + 0x28) + 0x80$.

Such as,

$$19^{\circ}\text{C}(\text{Fast update}) = 0x3b + 0x80 = 0xbb,$$

$$25^{\circ}\text{C}(\text{Fast update}) = 0x41 + 0x80 = 0xc1$$

*****The index value must be in the acceptable range, otherwise it will be abnormal*****

9. **TCON** is read from 0x0B of OTP memory.

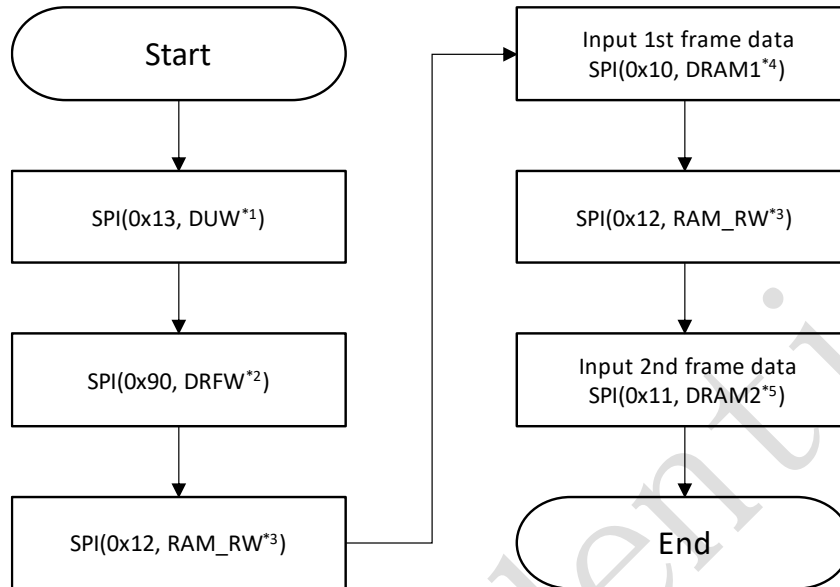
10. **STV_DIR** is read from 0x1B of OTP memory

11. **VCOM** is read from 0x11 of OTP memory

12. Please refer to section 3.3

3.2 Send image to the EPD

This section describes how to send image data into COG which will be displayed on the display. Since the display support both global update and partial.



Note:

- 1, **DUW**: there is 6 bytes' data that are read from 0x15 ~ 0x1A of OTP memory.
- 2, **DRFW**: there is 4 bytes' data that are read from 0x0C ~ 0x0F of OTP memory.
- 3, **RAM_RW**: there is 3 bytes' data that are read from 0x12 ~ 0x14 of OTP memory.
- 4, **DRAM1**: the data is the NEW image data that you want displaying next moment. its amount is 23,040 bytes.

- 5, **DRAM2**: The data definition of DRAM2 is different between "Normal update" and "Fast update".

Normal update: DRAM2 image is dummy data. It just needs to be filled with the enough amount of 0x00.

Fast update: DRAM2 image is the OLD image data that already displayed on the EPD.

EPD needs to receive both First and Second frame data each updating. The index of the First frame is **0x10** and the Second frame is **0x11**.

- Image format

The data of image frame, one bit represents 1 pixel. (e.g. the first byte represents the 1st~ 8thpixels of the first line, the second byte represents the 9th~ 16thpixels of the first line, and so on).

| | | | | | | | | |
|-----------|------|--------|--------|--------|--------|--------|--------|--------|
| Data Byte | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
| Pixel | P[n] | P[n+1] | P[n+2] | P[n+3] | P[n+4] | P[n+5] | P[n+6] | P[n+7] |

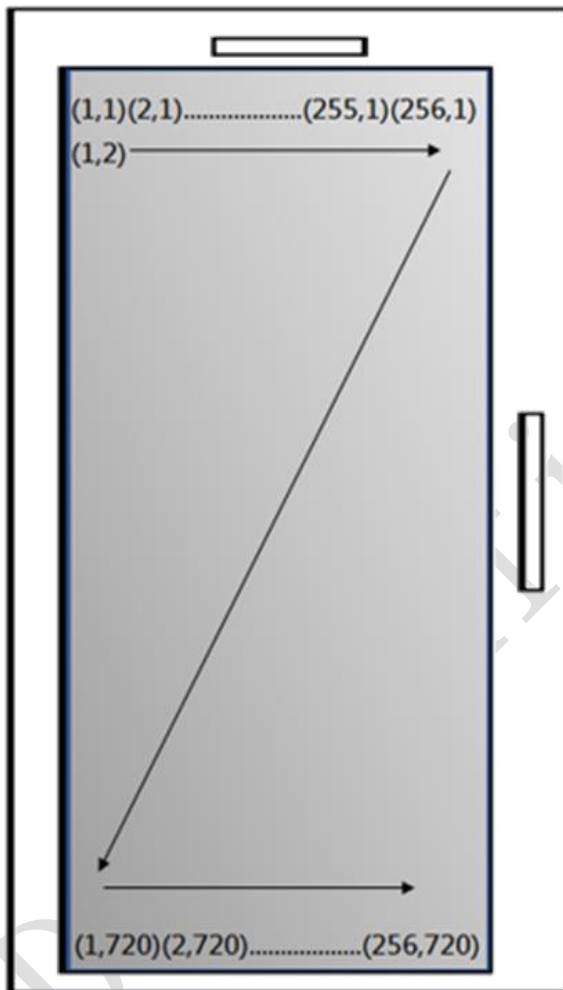


Image data input sequence:

Line1:(1,1)>(2,1)>...>(256,1)>

Line2:(1,2)>(2,2)>...>(256,2)>

⋮

⋮

⋮

⋮

⋮

Line720:.....>(256,720)>

Total:1 x 256 x 720

=184,320 bits

=23,040 Bytes

| Data | Pixel Color |
|------|-------------|
| 1 | Black |
| 0 | White |

- First frame

In this frame, the data is the NEW image data(DRAM1) that you want displaying next moment. The data "1" represents black color pixel and the data "0" represents both white color pixel.

| Data | Pixel Color |
|------|-------------|
| 1 | Black |
| 0 | White |

- Second frame

Normal update: DRAM2 image is dummy data. It just needs to be filled 23,040 bytes 0x00.

Fast update: DRAM2 image is the OLD image data that already displayed on the EPD.

3.3 DC/DC soft-start

There are 32-bytes data for describing the sequence of soft-start.

| | | | | | | | | |
|------|-----------|-----|------|------|------|------|------|------|
| | 0/8 | 1/9 | 2/10 | 3/11 | 4/12 | 5/13 | 6/14 | 7/15 |
| ... | | | | | | | | |
| 0x28 | 1st stage | | | | | | | |
| 0x30 | 2nd stage | | | | | | | |
| 0x38 | 3rd stage | | | | | | | |
| 0x40 | 4th stage | | | | | | | |
| ... | | | | | | | | |

The sequence totally has 4 stages. Each stage has 8 byte parameters. The bytes of each stage can be interpreted in 2 ways.

Data structure and definition:

| | 1st byte | 2nd byte | 3rd byte | 4th byte | 5th byte | 6th byte | 7th byte | 8th byte |
|---------|---------------|----------|----------|----------|----------|----------|----------|----------|
| format1 | REPEAT/FORMAT | PHL_INI | PHH_INI | PHL_VAR | PHH_VAR | BST_SW_a | BST_SW_b | DELAY |
| format2 | REPEAT/FORMAT | BST_SW_a | BST_SW_b | DELAY_a | DELAY_b | ? | ? | ? |

REPEAT/FORMAT:

The times to repeat and the data format used in this stage

The MSB defines the format used in this stage

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|--------|---|-----------------|---|---|---|---|---|
| REPEAT/FORMAT | Format | | Times to repeat | | | | | |

Format: 1-> bytes are defined as "format1"(see above)

0-> bytes are defined as "format2"(see above)

Example: 0x87 -> format1, repeat 7 times

0x64 -> format2, repeat 100 times

PHL_INI:

Define the initial value of PHL(the first data of the reg.0x51)

PHH_INI:

Define the initial value of PHH(the second data of the reg.0x51)

PHL_VAR:

The byte represents the changing value of PHL with each iteration(REPEAT)

PHH_VAR:

The byte represents the changing value of PHH with each iteration(REPEAT)

Both PHL_VAR_n and PHH_VAR_n could be a negative number. The negative number is represented by 2's complement.

Example: -5 equals 0xFB

BST_SW_a:

BST_SW setting is the power on/off manager(reg.0x09) at the start of the phase.

BST_SW_b:

BST_SW setting is the power on/off manager(reg.0x09) at the end of the phase.

DELAY:

The delay time at the end of the stage.

| | | | | | | | | |
|---------|-------|------------|---|---|---|---|---|---|
| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DELAY_n | Scale | Delay time | | | | | | |

Scale: 1 -> the scale of the delay time is msec.

0 -> the scale of the delay time is 10usec.

Example: 0x82 -> delay 2ms

0x02 -> delay 20us

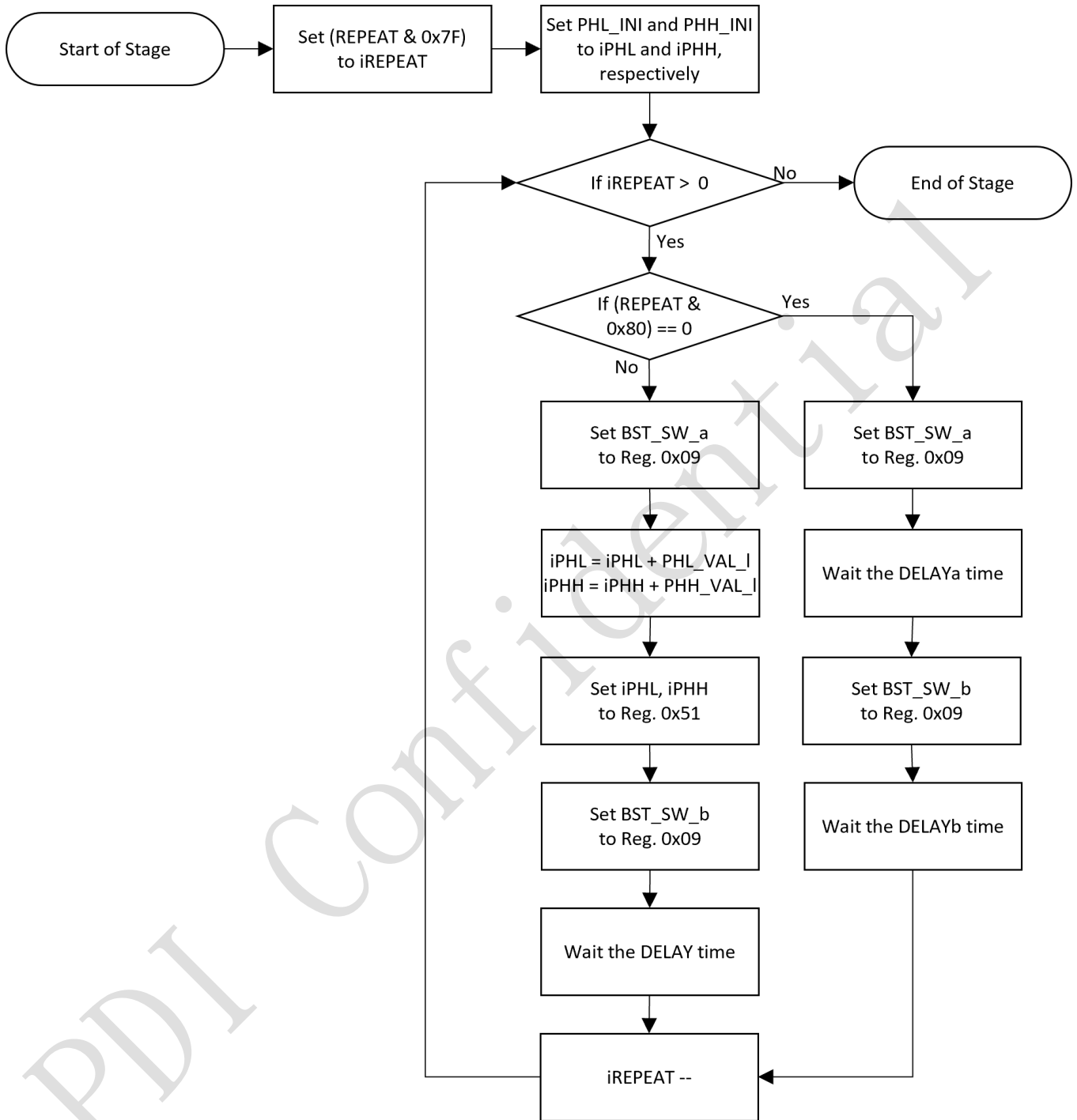
DELAY_a:

Same as "DELAY" but inserted after BST_SW_a

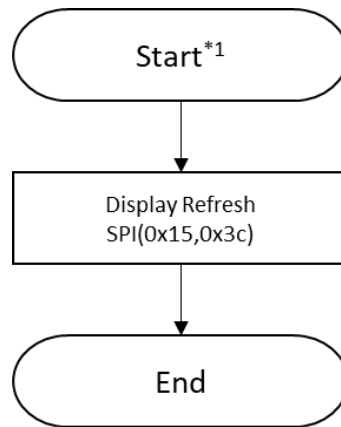
DELAY_b:

Same as "DELAY" but inserted after BST_SW_b

Following is the flowchart for each "stage",



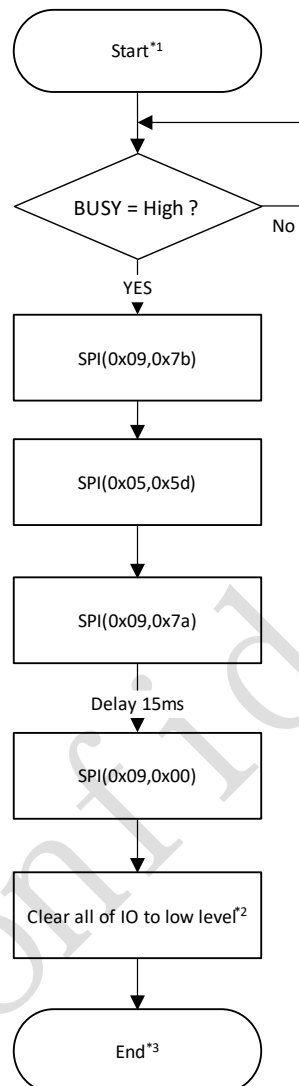
4 Send updating command



Note:

1. **Start:** Follow the end of the COG initial flow

5 Turn-off DC/DC



Note:

1. Start
Follow the end of the send updating command
2. VCC/VDD, RESETB, DC, CSB, SCL and SDA
3. Finished the all of the steps for update the 5.8" EPD

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Revision History

| Version | Date | Page (New) | Section | Description |
|---------|------------|------------|---------|------------------------------------|
| 01 | 2022/12/22 | | | First issue |
| 02 | 2023/2/6 | | 1.7 | Add 0x17 Flags define. |
| | | | 3.1 | Modify Temp & FU_IDX setting rule. |
| | | | 3.3 | Modify flowchat. |
| | | | | |
| | | | | |

Glossary of Acronyms

| | |
|-----------|---|
| EPD | Electrophoretic Display (e-Paper Display) |
| EPD Panel | EPD |
| TCon | Timing Controller |
| FPL | Front Plane Laminate (e-Paper Film) |
| SPI | Serial Peripheral Interface |
| COG | Chip on Glass |
| PDI, PDi | Pervasive Displays Incorporated |

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