Application Note
for
Wide Temperature EPD
(Dual Chip)

Description	**Interface for the Wide Temperature EPD (Dual Chip)**
Date	**2023/8/4**
Doc. No.	
Revision	**01**

4F, No. 28, Chuangye Rd., Tainan Science Park, Tainan City 74144, Taiwan (R.O.C.)
Tel: +886-6-279-5399 Fax: +886-6-270-5857

Table of Contents

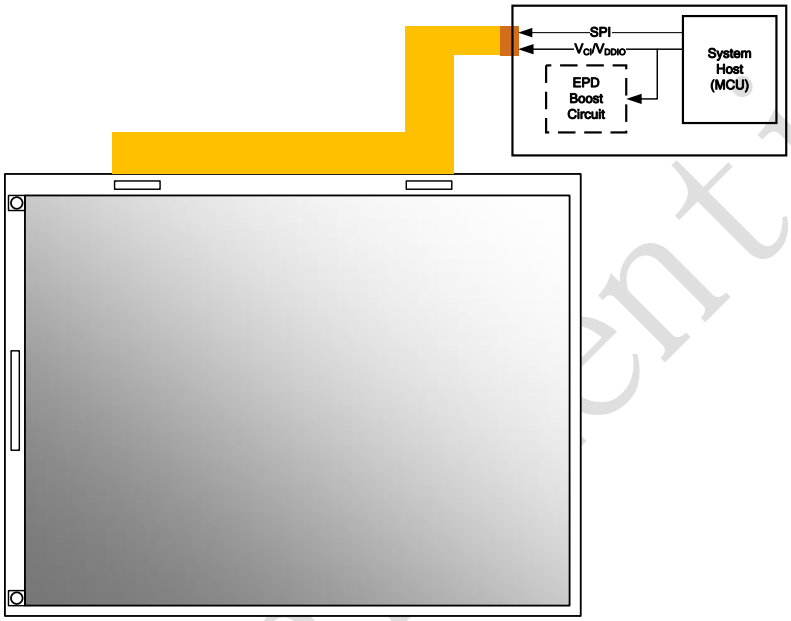
1 General Description

1.1 Overview

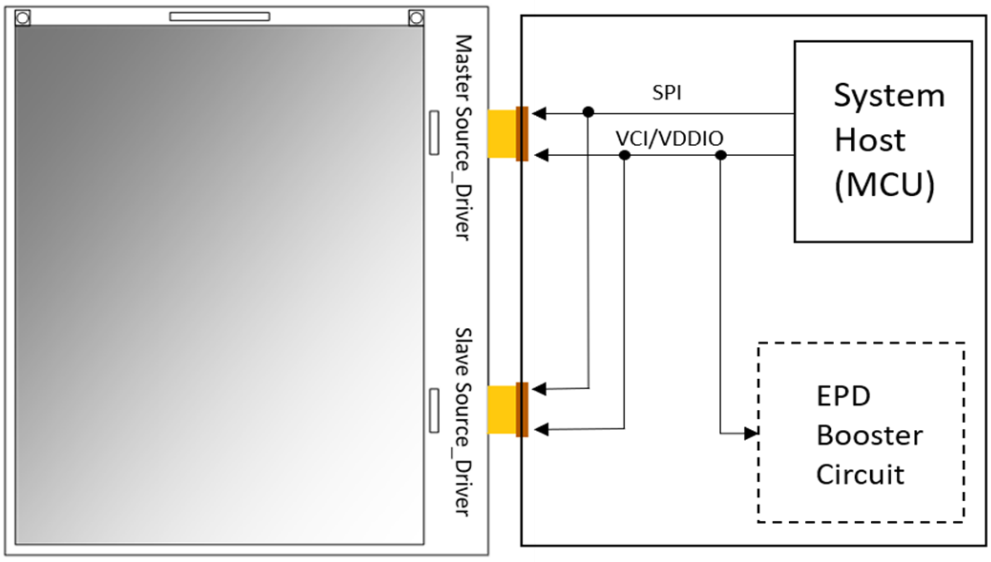
The document introduces how to drive the EPD with the new generation driver chip.

They include the **9.7" ,12" inch**. The EPD has embedded the Tcon function. The major control interface of the driver is SPI. The host sends both the setting commands and the display image to driver through the SPI bus.

(Single FPC)



(Dual FPC)



1.2 Definition of operation mode

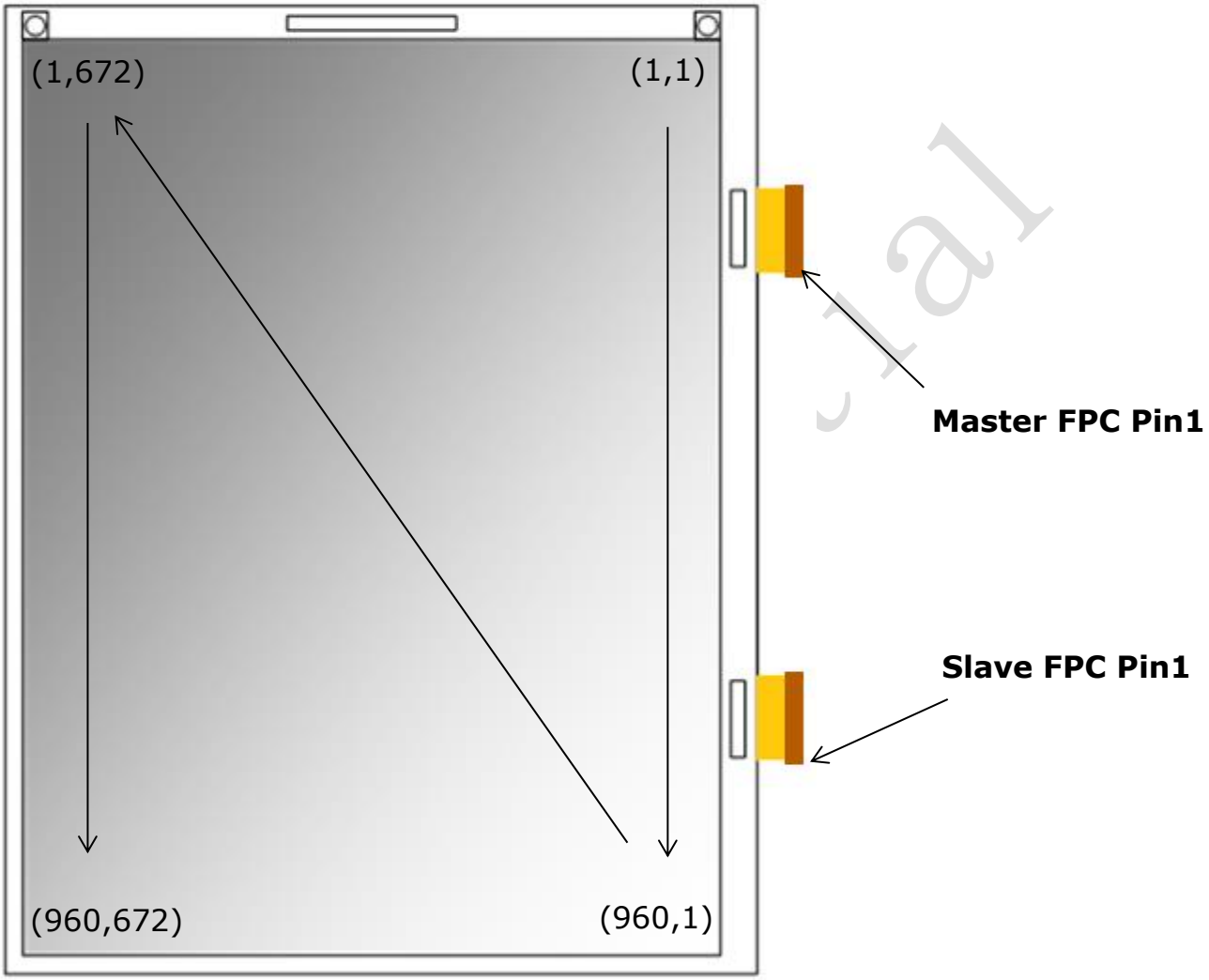
The section will define and clarify update modes.

Normal update: it will perform the complete waveform for image update. The process will go through the inverse, shaking and imaging phases. The mode will take more time, but it will bring better image performance.

Fast update: the short waveform will be executed. COG compares the pixel data of the current image and the new image pixel by pixel, and then only drives the transition pixels. The mode can quickly complete the image update.

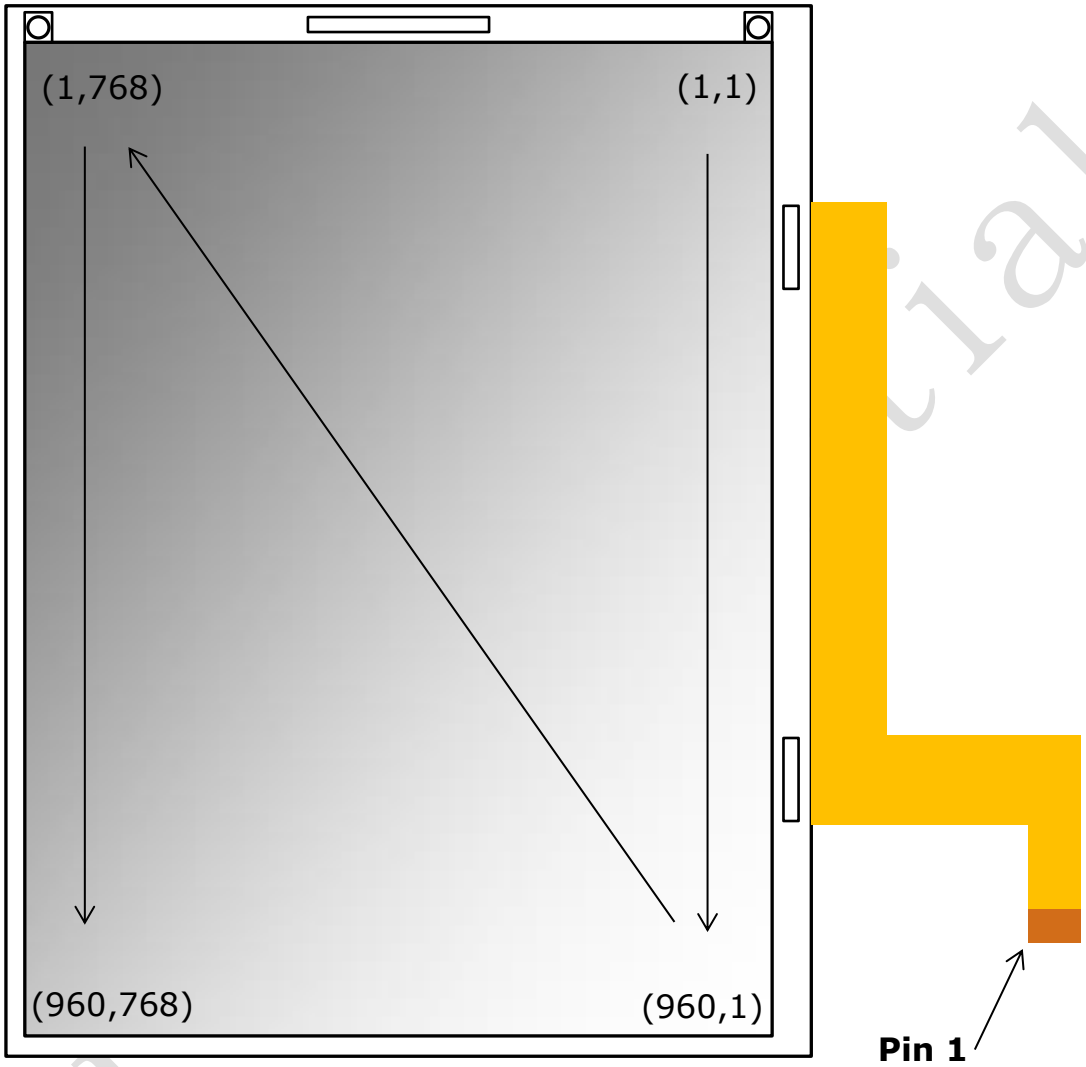
1.3 Panel drawing

9.7-inch EPD

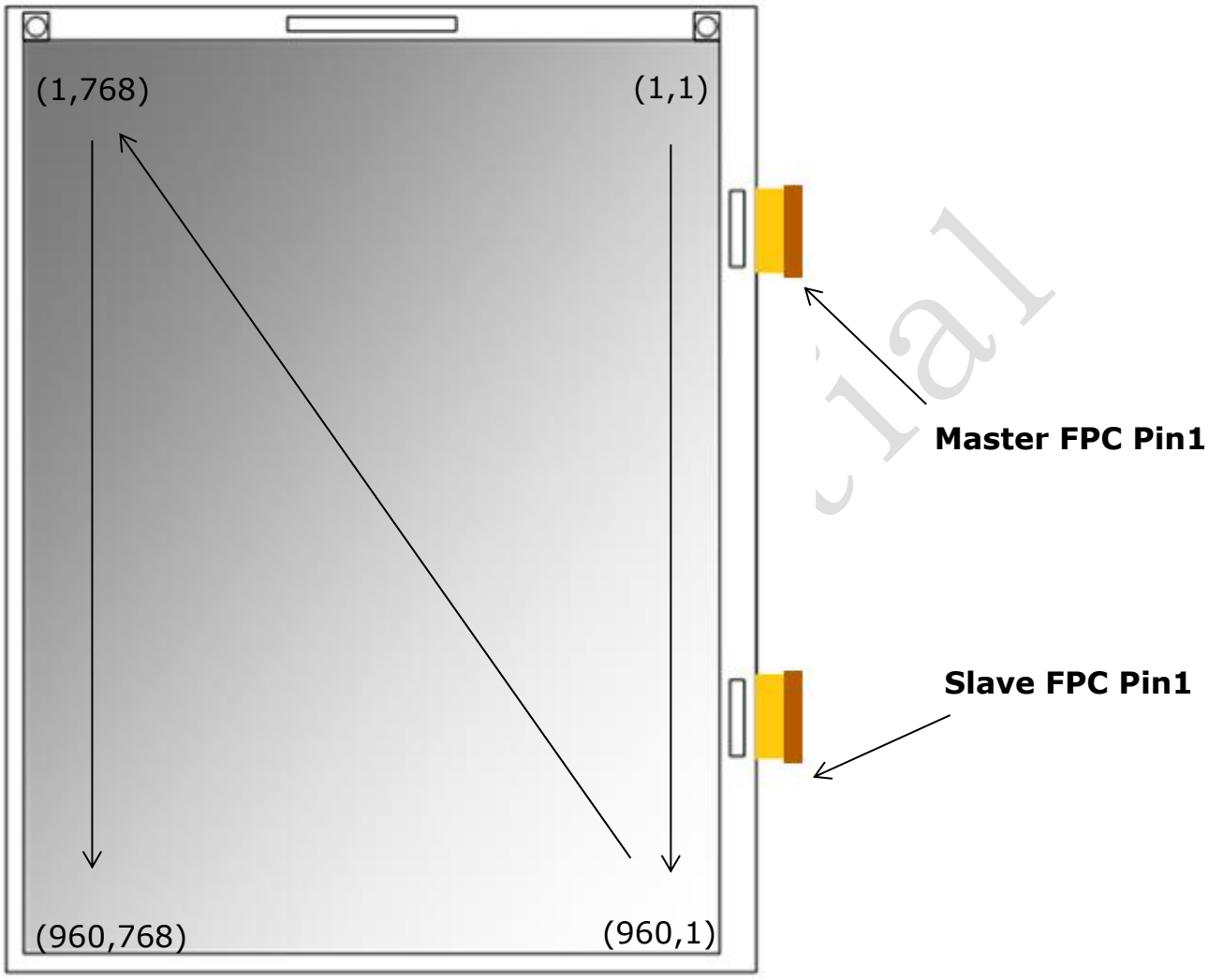


12-inch EPD

(Single FPC)



(Dual FPC)

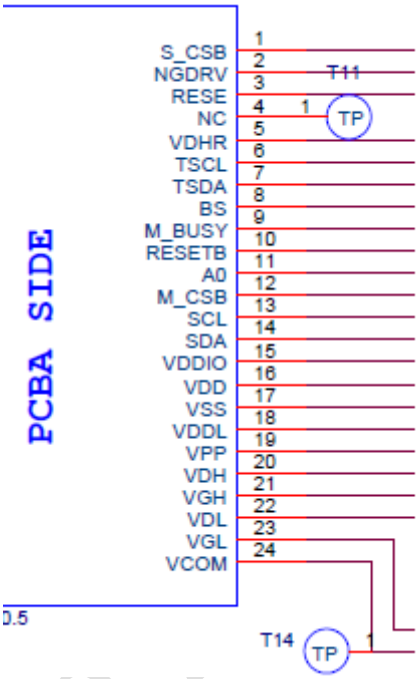


1.4 EPD Interface

The Dual EPD was mounted two source drivers. They are Master and Slave role respectively and share the same SPI with separate CS.

The pin assignment of FPC are as follows, the pitch of FPC is 0.5mm.

(Single FPC)



The 12th pin, M_CSB is the CS of Master. The first pin, S_CSB is the CS of Slave.

(Dual FPC)

1.4-1 Master FPC Pin Define

No.	Signal	Type	Connected to	Function
1	FSYNC	I/O	Slave FSYNC	Cascade line frame sync
2	NGDRV	O	Power MOSFET Driver control	This pin is the N-Channel MOSFET Gate Drive Control.
3	RESE	I	Booster Control Input	This pin is the Current Sense Input for the Control Loop.
4	INTERNAL_VPP	P	VPP PIN & Slave FPC	OTP power internal
5	VDHR	C	Capacitor	This pin is the VDHR driving voltage. A stabilizing capacitor should be connected between VDHR and VSS.
6	LNSYNC	I/O	Slave LNSYNC	Cascade line sync
7	CLK	I/O	Slave CLK	Cascade clock
8	BS	I	VSS	This pin is setting panel interface.
9	M_BUSY	O	Device Busy Signal	This pin is Busy state output pin of the master chip. When Busy is Low, the operation of the chip should not be interrupted, and Command should not be sent.
10	RESETB	I	System Reset	This pin is reset signal input. Active Low.
11	A0	I	VDDIO or VSS	This pin is Data/Command control.
12	M_CSB	I	VDDIO or VSS	This pin is the Master chip select.
13	SCL	I	Data Bus	Serial communication clock input.
14	SDA	I	Data Bus	Serial communication data input/output.
15	VDDIO	P	Power Supply	Power for interface logic pins & I/O. It should be connected with VDDIO.
16	VDD	P	Power Supply	Power Supply for the chip.
17	VSS	P	Ground	Ground
18	VDDL	C	Capacitor	Internal regulator output A capacitor should be connected between VDDL and VSS.
19	VPP	P	INTERNAL_VPP& Slave VPP	OTP power

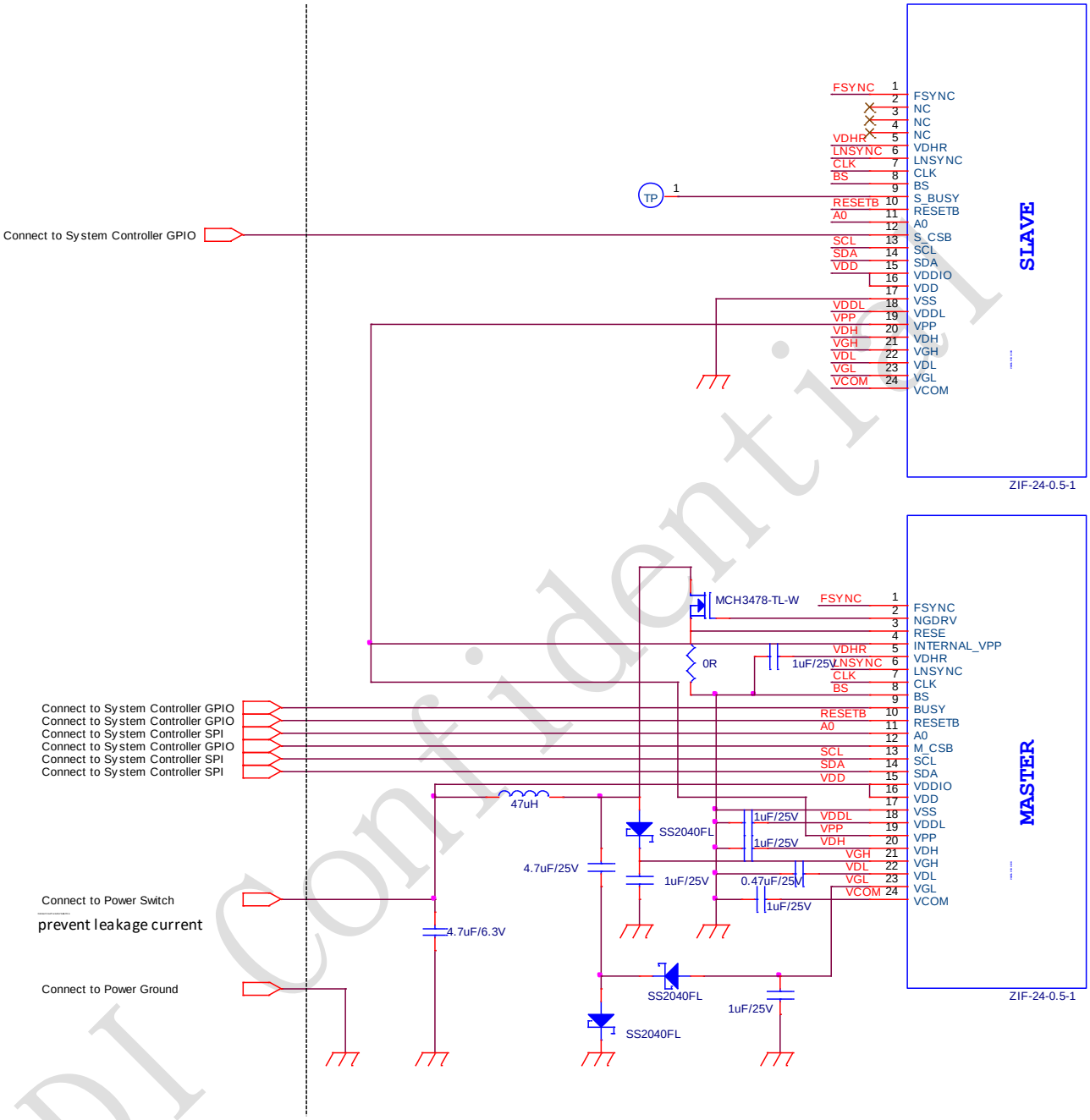
No.	Signal	Type	Connected to	Function
20	VDH	C	Capacitor	This pin is the Positive Source driving voltage. A stabilizing capacitor should be connected between VDH and VSS.
21	VGH	C	Capacitor	This pin is the Positive Gate driving voltage A stabilizing capacitor should be connected between VGH and VSS.
22	VDL	C	Capacitor	This pin is the Negative Source driving voltage. A stabilizing capacitor should be connected between VDL and VSS.
23	VGL	C	Capacitor	This pin is the Negative Gate driving voltage. A stabilizing capacitor should be connected between VGL and VSS.
24	VCOM	C	Capacitor	This pin is the VCOM driving voltage A stabilizing capacitor should be connected between VCOM and VSS.

1.4-2 Slave FPC Pin Define

No.	Signal	Type	Connected to	Function
1	FSYNC	I/O	Master FSYNC	Cascade line frame sync
2	NC	-	-	Not connected
3	NC	-	-	Not connected
4	NC	-	-	Not connected
5	VDHR	C	Capacitor	This pin is the VDHR driving voltage. A stabilizing capacitor should be connected between VDHR and VSS.
6	LNSYNC	I/O	Master LNSYNC	Cascade line sync
7	CLK	I/O	Master CLK	Cascade clock
8	BS	I	VSS	This pin is setting panel interface.
9	S_BUSY	O	Device Busy Signal	This pin is Busy state output pin of the slave chip. When Busy is Low, the operation of the chip should not be interrupted, and Command should not be sent.
10	RESETB	I	System Reset	This pin is reset signal input. Active Low.
11	A0	I	VDDIO or VSS	This pin is Data/Command control.
12	S_CSB	I	VDDIO or VSS	This pin is the Slave chip select.
13	SCL	I	Data Bus	Serial communication clock input.
14	SDA	I	Data Bus	Serial communication data input/output.

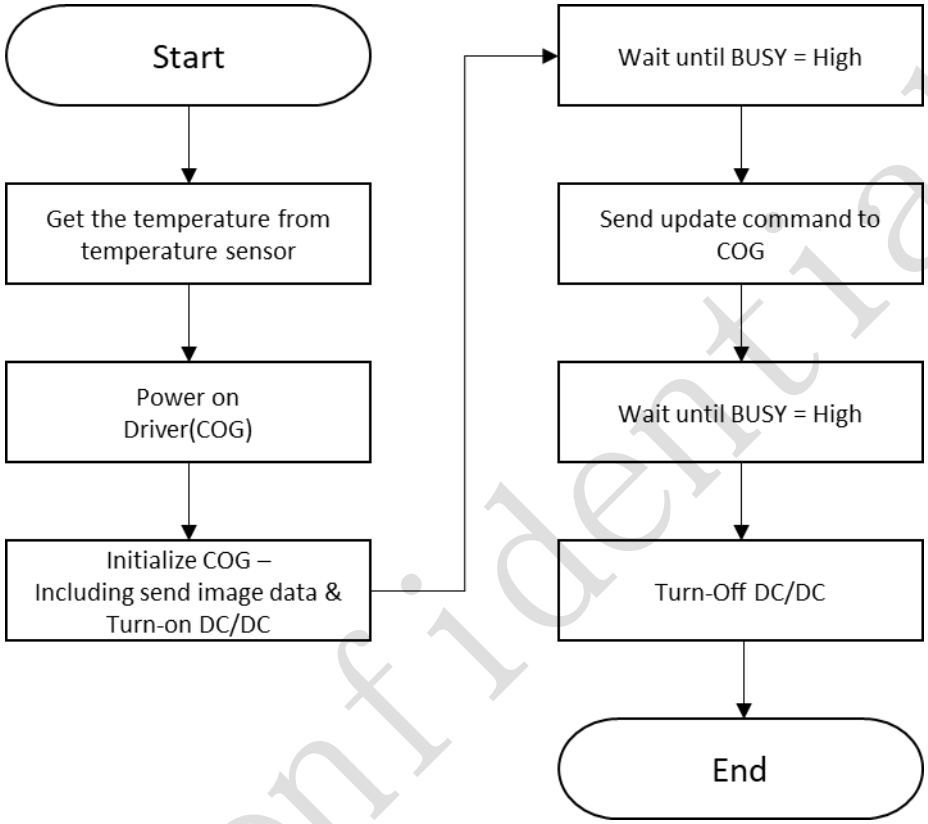
No.	Signal	Type	Connected to	Function
15	VDDIO	P	Power Supply	Power for interface logic pins & I/O. It should be connected with VDDIO.
16	VDD	P	Power Supply	Power Supply for the chip.
17	VSS	P	Ground	Ground
18	VDDL	C	Capacitor	Internal regulator output A capacitor should be connected between VDDL and VSS.
19	VPP	P	Master VPP	OTP power
20	VDH	C	Capacitor	This pin is the Positive Source driving voltage. A stabilizing capacitor should be connected between VDH and VSS.
21	VGH	C	Capacitor	This pin is the Positive Gate driving voltage A stabilizing capacitor should be connected between VGH and VSS.
22	VDL	C	Capacitor	This pin is the Negative Source driving voltage. A stabilizing capacitor should be connected between VDL and VSS.
23	VGL	C	Capacitor	This pin is the Negative Gate driving voltage. A stabilizing capacitor should be connected between VGL and VSS.
24	VCOM	C	Capacitor	This pin is the VCOM driving voltage A stabilizing capacitor should be connected between VCOM and VSS.

1.4-3 EPD Reference Circuit



1.5 EPD Driving Flow Chart

The flowchart below provides an overview of the necessary actions to update the EPD. The steps below refer to the detailed descriptions in the respective sections.



1.6 SPI Timing Format

SPI commands are used to communicate between the MCU and the COG Driver. The SPI format used differs from the standard in that two way communications are not used. When setting up the SPI timing, PDI recommends verify both the SPI command format and SPI command timing in this section.

The maximum clock speed of the display is **20MHz(Write), 2.5MHz(Read)**.

- Below is a description of the SPI Format:

  SPI(0xI, $0xD_1$, $0xD_2$, …, $0xD_n$, csDS)

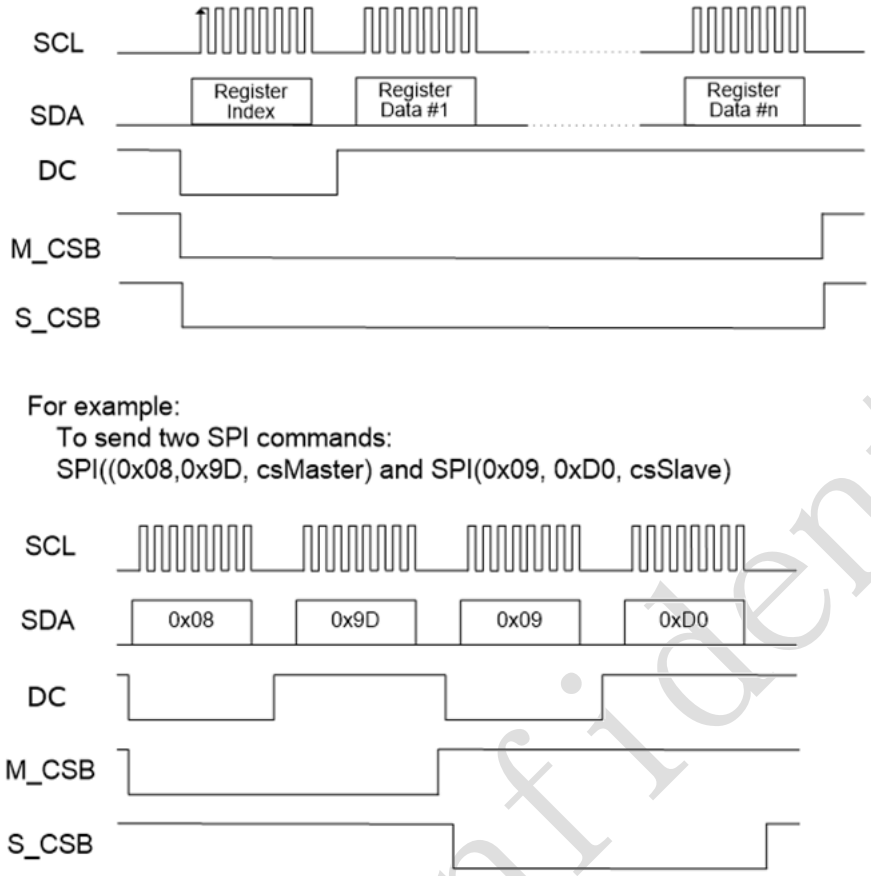
  Where:

  I is the Register Index and the length is 1 byte
  $D_{1\sim n}$ is the Register Data. The Register Data length is variously.

  The csDS indicates this command is delivered to which driver or both.
  csMaster : only deliver to Master driver
  csSlave : only deliver to Slave driver
  csBoth : deliver to both Master and Slave

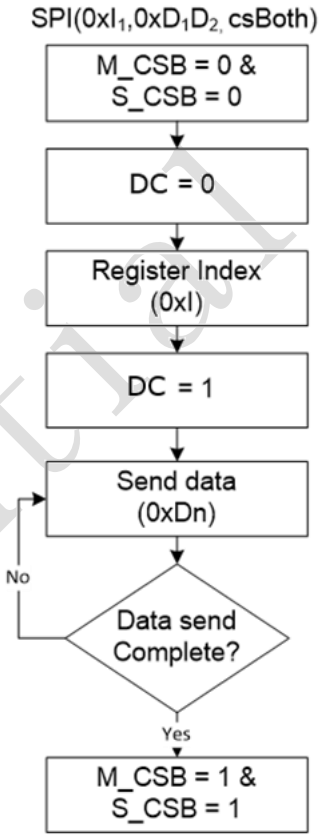
- When SPI sends the Index, the DC has to pull LOW. When sends the data, the DC has to pull HIGH. The next page is the detail flow chart.

- SPI command signals and flowchart:



For example:
To send two SPI commands:
SPI((0x08,0x9D, csMaster) and SPI(0x09, 0xD0, csSlave)

If register data is larger than two bytes, you must input data continuously without setting Register Index again.

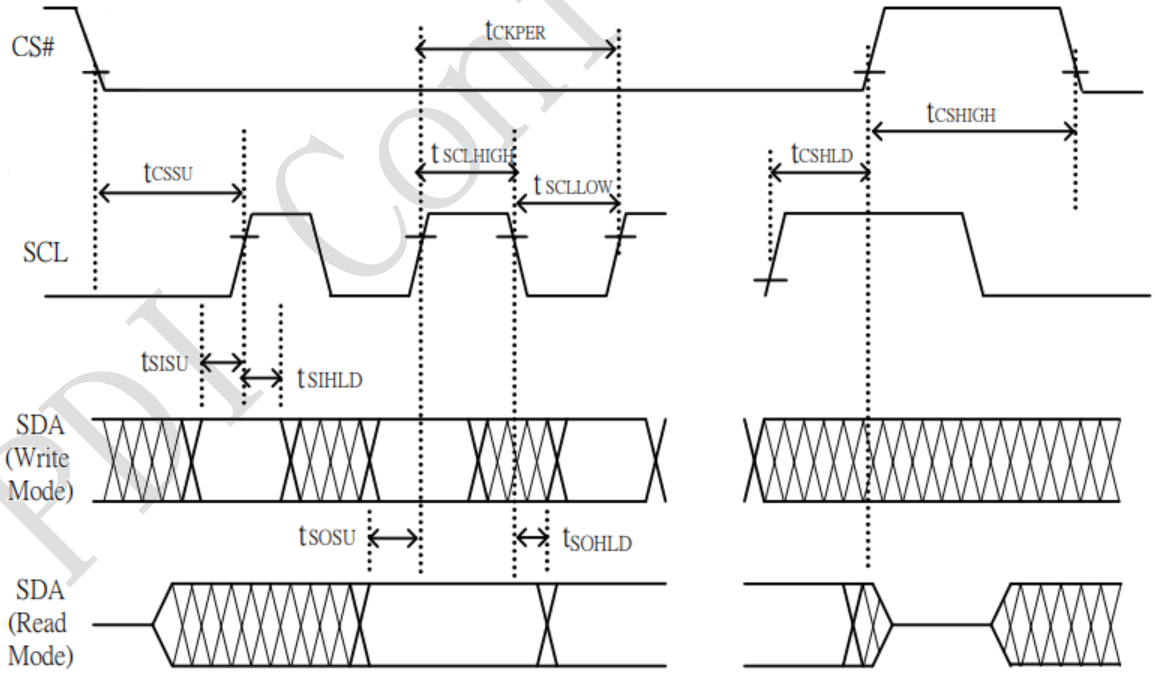


- SPI command timing

The following specifications apply for: VDDIO - GND = 2.3V to 3.6V, TOPR = 25°C, CL=20pF

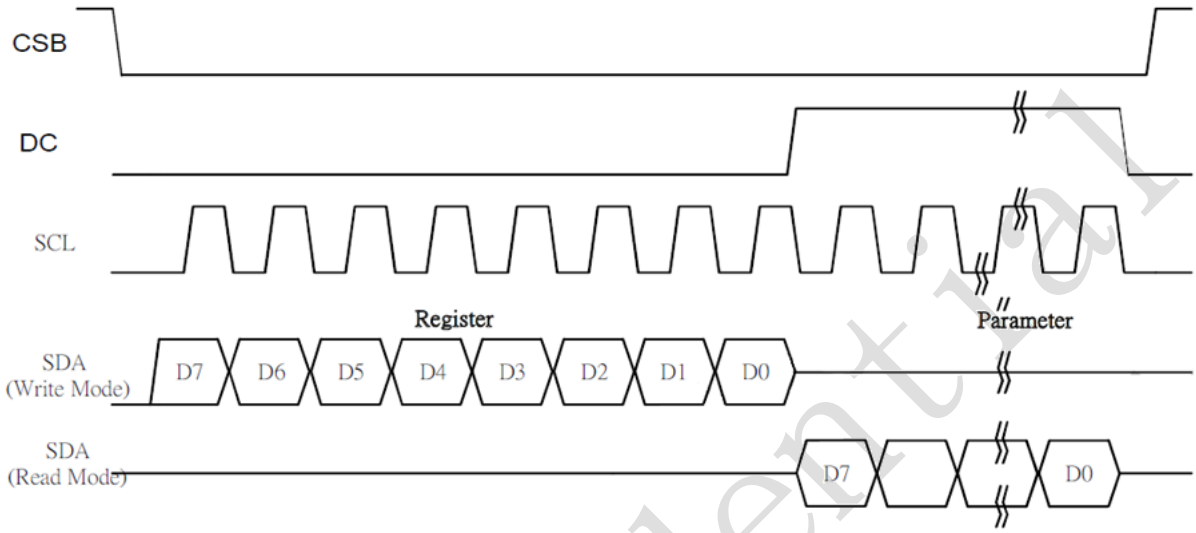
Item	Symbol	Min.	Typ.	Max.	Unit
SCL frequency (Write Mode)	f_{SCL}	-	-	20	MHz
Time CSB has to be low before the first rising edge of SCLK	t_{CSSU}	60	-	-	ns
Time CSB has to remain low after the last falling edge of SCLK	t_{CSHLD}	65	-	-	ns
Time CSB has to remain high between two transfers	t_{CSHIGH}	100	-	-	ns
Part of the clock period where SCL has to remain high	$t_{SCLHIGH}$	25	-	-	ns
Part of the clock period where SCL has to remain low	t_{SCLLOW}	25	-	-	ns
Time SI has to be stable before the next rising edge of SCL	t_{SISU}	10	-	-	ns
Time SI has to remain stable after the rising edge of SCL	t_{SIHLD}	40	-	-	ns

Item	Symbol	Min.	Typ.	Max.	Unit
SCL frequency(Read Mode)	f_{SCL}	-	-	2.5	MHz
Time CSB has to be low before the first rising edge of SCLK	t_{CSSU}	100	-	-	ns
Time CSB has to remain low after the last falling edge of SCLK	t_{CSHLD}	50	-	-	ns
Time CSB has to remain high between two transfers	t_{CSHIGH}	250	-	-	ns
Part of the clock period where SCL has to remain high	$t_{SCLHIGH}$	180	-	-	ns
Part of the clock period where SCL has to remain low	t_{SCLLOW}	180	-	-	ns
Time SO will be stable before the next rising edge of SCL	t_{SOSU}	-	50	-	ns
Time SO will remain stable after the rising edge of SCL	t_{SOHLD}	-	0	-	ns



1.7 Read OTP data

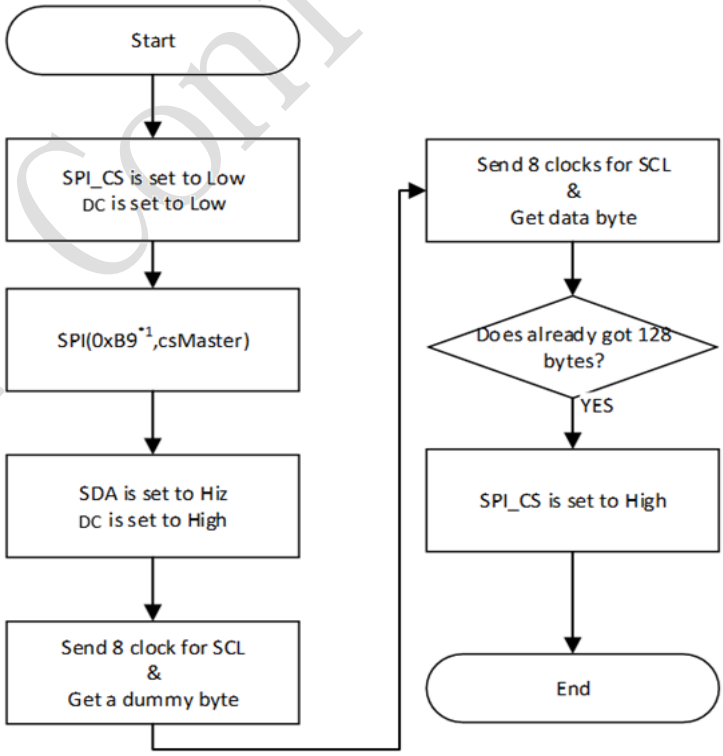
The 128-bytes section of OTP have saved the user-defined data that includes the information of the display and soft-start parameters. The section will introduce how to read out the data through the SPI.



Note: 1. After read enable command is set, SDA must set Hiz, and DC set high to active read operation

2. When read operation is done, CSB must set high once to quit read operation.

Read operation of 4-Line SPI



1.8 User-defined data

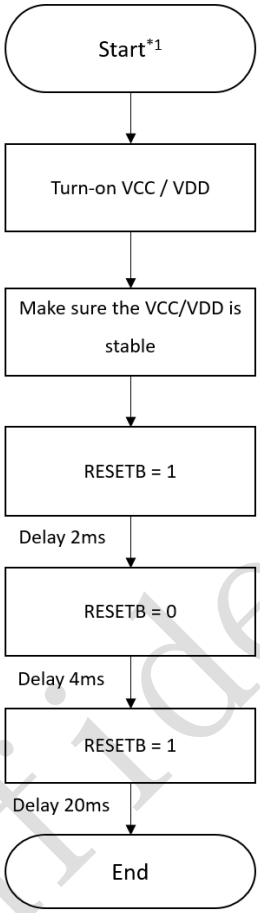
User's firmware needs to read out the user-defined data with 0xB9 command, and to initialize the COG with the parameters.

ADDR	CONTENT	BYTE
0x00	Reserved	1 Byte
0x01	COG Type	1 Byte
0x02	Vender	1 Byte
0x03	Waveform Rev	1 Byte
0x04 | 0x09	FPL lot name (6 bytes of ACSII characters)	6 Byte
0x0A	Color	1 Byte
0x0B	TCON	1 Byte
0x0C	DRFW0	1 Byte
0x0D	DRFW1	1 Byte
0x0E	DRFW2	1 Byte
0x0F	DRFW3	1 Byte
0x10	DCTL	1 Byte
0x11	VCOM	1 Byte
0x12	RAM R/W Start 0	1 Byte
0x13	RAM R/W Start 1	1 Byte
0x14	RAM R/W Start 2	1 Byte
0x15	DUW 0	1 Byte
0x16	DUW 1	1 Byte
0x17	DUW 2	1 Byte
0x18	DUW 3	1 Byte
0x19	DUW 4	1 Byte
0x1A	DUW 5	1 Byte
0x1B	STV_DIR	1 Byte
0x1C	MS_SYNC	1 Byte
0x1D	BVSS	1 Byte
0x1E	Flags	1 Byte
0x1F	VCOM_CTRL	1 Byte
0x20 | 0x27	Reserved	8 Byte
0x28 | 0x2F	Stage 1 of the booster boot sequence	8 Byte
0x30 | 0x37	Stage 2 of the booster boot sequence	8 Byte
0x38 | 0x3F	Stage 3 of the booster boot sequence	8 Byte
0x40 | 0x47	Stage 4 of the booster boot sequence	8 Byte
0x48 | 0x7F	Reserved	56 Byte

COG Type(0x01): 0x96 -> dual-chip
Vendor(0x02): 0x01 -> PDI
Waveform Rev.(0x03): revision of the waveform
FPL lot name(0x04~0x09): Display FPL-LOT number with 6-character ASCII
Color(0x0A): 0x00 -> Black/White
Flags(0x1E): 0xFE -> Fast update is supported.
Others(0x0B ~ 0x47): the area data will be used on initial process. They will be mentioned on following sections.

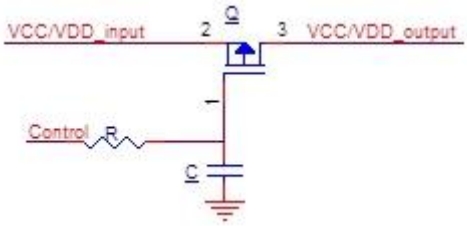
2 Power on COG driver

This flowchart describes power sequence for driver chip.



Note:

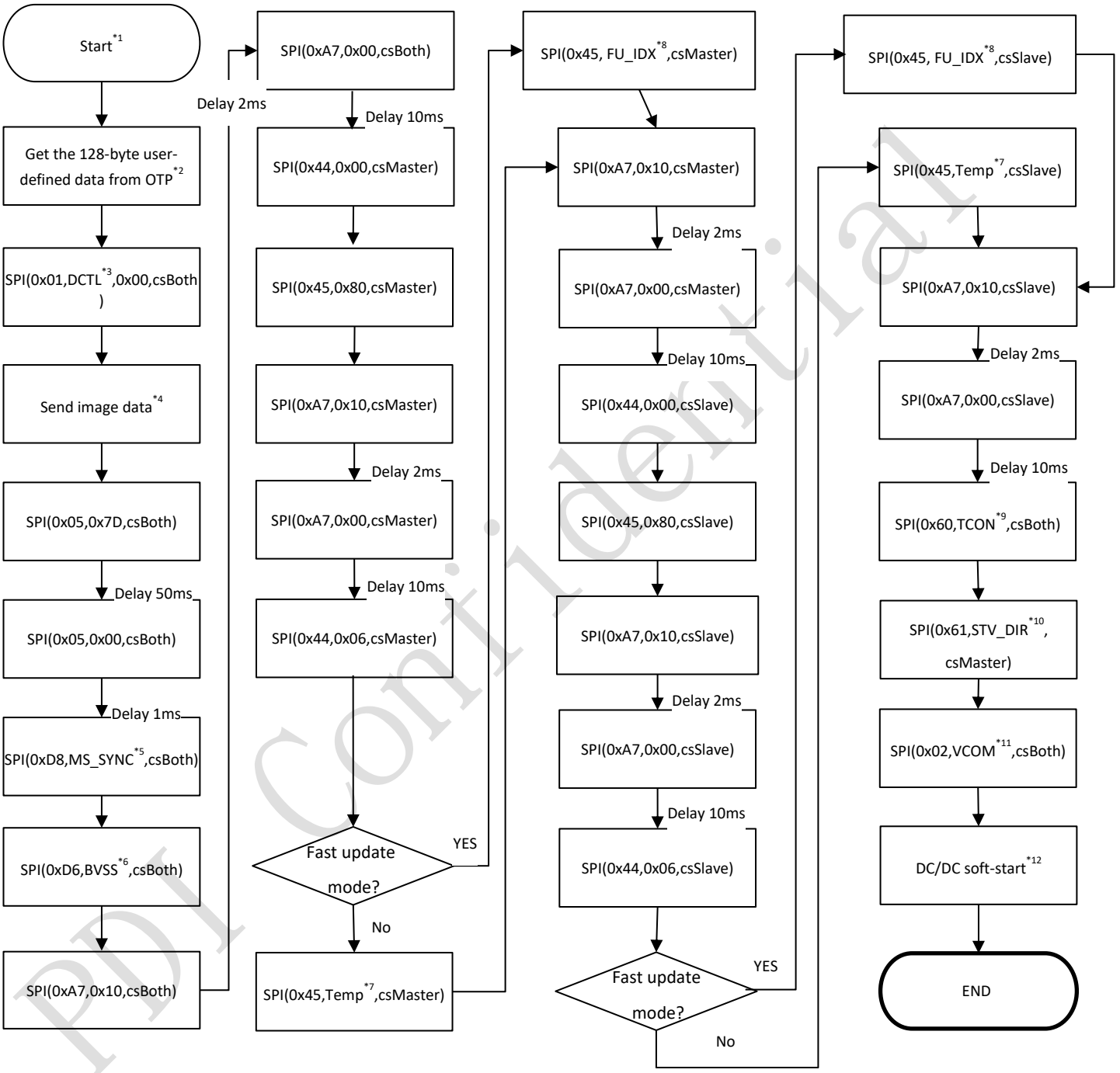
1. **Start:** is the initial state. VCC/VDD, RESETB, CSB_M, CSB_S, SDA, SCL must be kept at 0v. In order to the inrush current will cause other issue. It is recommended to add soft-start when VCC/VDD is turned on.



VCC/VDD soft-start

3 Initialize COG Driver

3.1 Initial flow chart



Note:

1. **Start:** Follow the end of the power on sequence
2. Please refer to section 1.7 to get the 128-bytes of the user-defined.
3. **DCTL** is read from 0x10 of OTP memory (section1.7)
4. Please refer to section 3.2
5. **MS_SYNC** is read from 0x1C of OTP memory(section1.7)
6. **BVSS** is read from 0x1D of OTP memory(section1.7)
7. **Temp** is an index of the **Normal Update**. The acceptable range of temperature is

-15℃ ~ 60℃ and 1℃ per step. **Temp** = temperature + 0x28.
Such as,

-15°C = 0x19,
0°C = 0x28,
25°C = 0x41,
60°C = 0x64

If temperature higher than 60°C, just set to 0x64.(Normal Update)
If temperature lower than -15°C, just set to 0x25.(Normal Update)

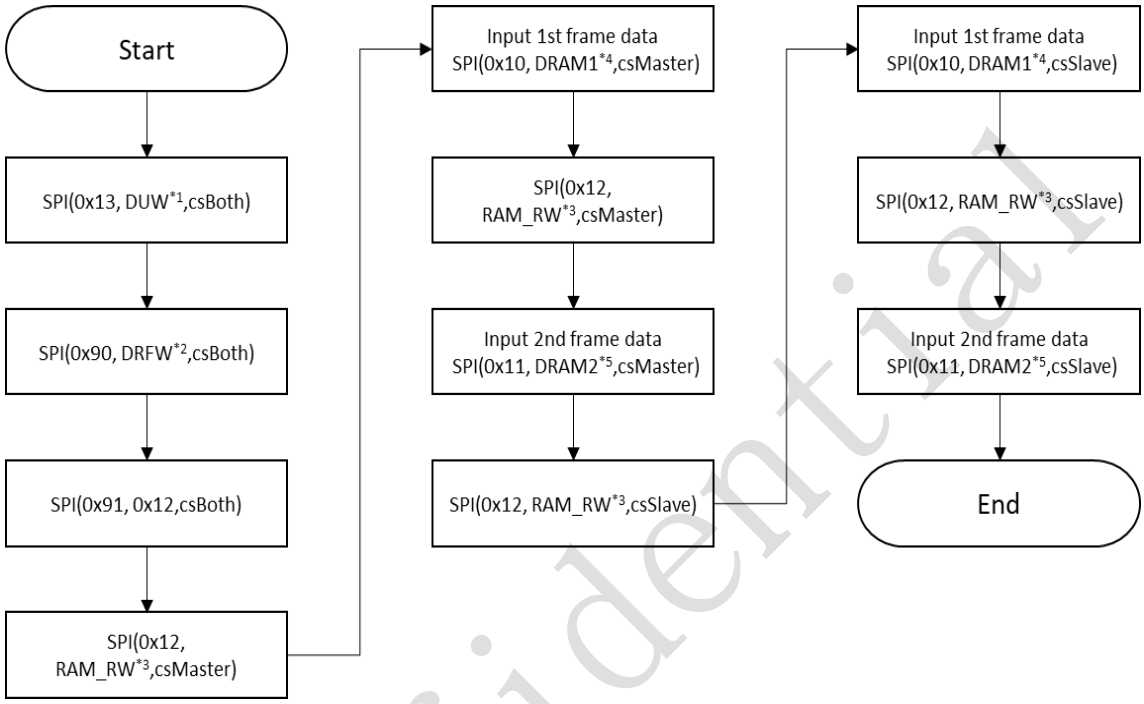
8. **FU_IDX** is an index of the **Fast Update**. The acceptable range of temperature is 0℃ ~ 50℃ and 1℃ per step. **FU_IDX** = (temperature + 0x28) + 0x80.
   Such as,
   19°C(Fast update) = 0x3b + 0x80 = 0xbb,
   25°C(Fast update) = 0x41 + 0x80 = 0xc1

If temperature higher than 50°C, just set to 0xda.(Fast Update)
If temperature lower than 0°C, just set to 0xa8.(Fast Update)
The index value must be in the acceptable range, otherwise it will be abnormal

9. **TCON** is read from 0x0B of OTP memory.
10. **STV_DIR** is read from 0x1B of OTP memory
11. **VCOM** is read from 0x11 of OTP memory
12. **VCOM_CTRL** is read from 0x1F of OTP memory
13. Please refer to section 3.3

3.2 Send image to the EPD

This section describes how to send image data into COG which will be displayed on the display. Since the display support both Normal Update and Fast Update.



Note:

1. **DUW:** there is 6 bytes' data that are read from 0x15 ~ 0x1A of OTP memory.
2. **DRFW:** there is 4 bytes' data that are read from 0x0C ~ 0x0F of OTP memory.
3. **RAM_RW:** there is 3 bytes' data that are read from 0x12 ~ 0x14 of OTP memory.
4. **DRAM1**: the data is the NEW image data that you want displaying next moment. its amount the follow bytes.

9.7-inch	40,320 bytes
12-inch	46,080 bytes

5. **DRAM2**: The data definition of DRAM2 is different between "Normal update" and "Fast update".

   Normal update: DRAM2 image is dummy data. It just needs to be filled with the enough amount of 0x00.

   Fast update: DRAM2 image is the OLD image data that already displayed on the EPD.

EPD needs to receive both First and Second frame data each updating. The index of the First frame is **0x10** and the Second frame is **0x11.**

- Image format

The data of image frame, one bit represents 1 pixel. (e.g. the first byte represents the 1st~ 8thpixels of the first line, the second byte represents the 9th~ 16thpixels of the first line, …… and so on).

Data Byte	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Pixel	P[n]	P[n+1]	P[n+2]	P[n+3]	P[n+4]	P[n+5]	P[n+6]	P[n+7]

9.7”

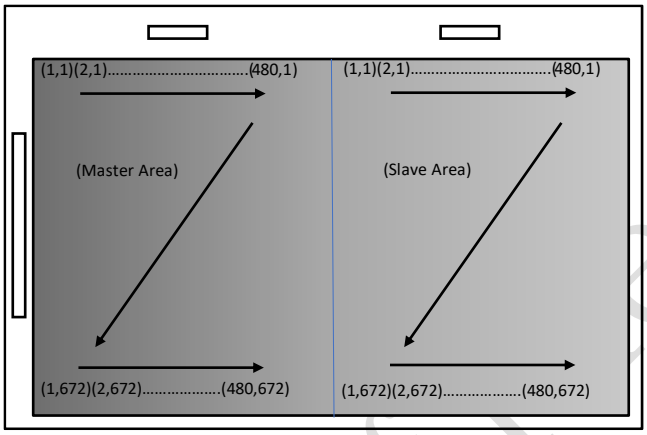
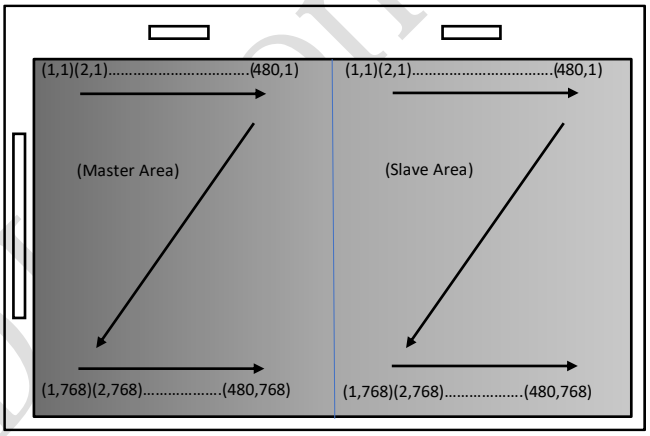


Image data input sequence:
Line1:(1,1)>(2,1)>…>(N,1)>
Line2:(1,2)>(2,2)>…>(N,2)>
.
.
.
LineM: ..... >(N,M)>

12”



EPD size	N	M
9.7”	480	672
12”	480	768

Data	Pixel Color
1	Black
0	White

- First frame

  In this frame, the data is the NEW image data(DRAM1) that you want displaying next moment. The data "1" represents black color pixel and the data "0" represents both white color pixel.

Data	Pixel Color
1	Black
0	White

- Second frame

  Normal update: DRAM2 image is dummy data. It just needs to be filled the follow bytes 0x00.

9.7-inch	40,320 bytes
12-inch	46,080 bytes

Fast update: DRAM2 image is the OLD image data that already displayed on the EPD.

3.3 DC/DC soft-start

There are 32-bytes data for describing the sequence of soft-start.

	0/8	1/9	2/10	3/11	4/12	5/13	6/14	7/15
…	…….							
0x28	1st stage							
0x30	2nd stage							
0x38	3rd stage							
0x40	4th stage							
…	……							

The sequence totally has 4 stages. Each stage has 8 byte parameters. The bytes of each stage can be interpreted in 2 ways.

Data structure and definition:

	1st byte	2nd byte	3rd byte	4th byte	5th byte	6th byte	7th byte	8th byte
format1	REPEAT/FORMAT	PHL_INI	PHH_INI	PHL_VAR	PHH_VAR	BST_SW_a	BST_SW_b	DELAY
format2	REPEAT/FORMAT	BST_SW_a	BST_SW_b	DELAY_a	DELAY_b	?	?	?

REPEAT/FORMAT:

The times to repeat and the data format used in this stage

The MSB defines the format used in this stage

bit	7	6	5	4	3	2	1	0
REPEAT/FORMAT	Format	Times to repeat						

Format: 1-> bytes are defined as “format1”(see above)

0-> bytes are defined as “format2”(see above)

Example: 0x87 -> format1, repeat 7 times

0x64 -> format2, repeat 100 times

PHL_INI:

Define the initial value of PHL(the first data of the reg.0x51)

PHH_INI:

Define the initial value of PHH(the second data of the reg.0x51)

PHL_VAR:

The byte represents the changing value of PHL with each iteration(REPEAT)

PHH_VAR:

The byte represents the changing value of PHH with each iteration(REPEAT)

Both PHL_VAR_n and PHH_VAR_n could be a negative number. The negative number is represented by 2's complement.

Example: -5 equals 0xFB

BST_SW_a:

BST_SW setting is the power on/off manager(reg.0x09) at the start of the phase.

BST_SW_b:

BST_SW setting is the power on/off manager(reg.0x09) at the end of the phase.

DELAY:

The delay time at the end of the stage.

bit	7	6	5	4	3	2	1	0
DELAY_n	Scale	Delay time						

Scale: 1 -> the scale of the delay time is msec.

0 -> the scale of the delay time is 10usec.

Example: 0x82 -> delay 2ms

0x02 -> delay 20us

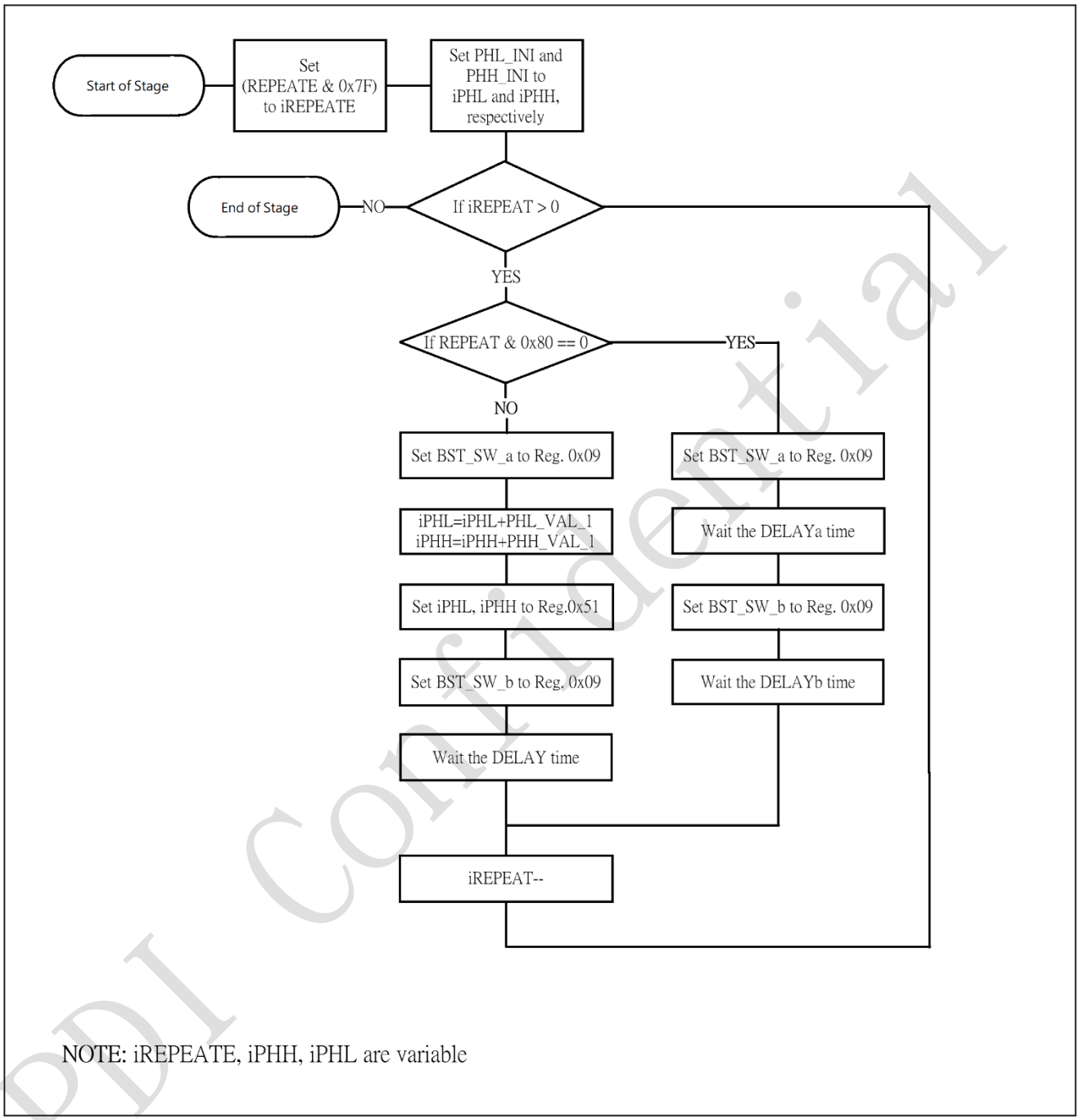
DELAY_a:

Same as "DELAY" but inserted after BST_SW_a

DELAY_b:

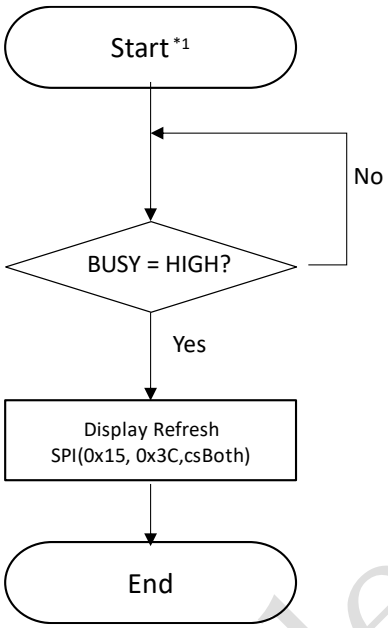
Same as "DELAY" but inserted after BST_SW_b

Following is the flowchart for each "stage". The following command must to send both Master and Slave COG.



NOTE: iREPEATE, iPHH, iPHL are variable

4 Send updating command

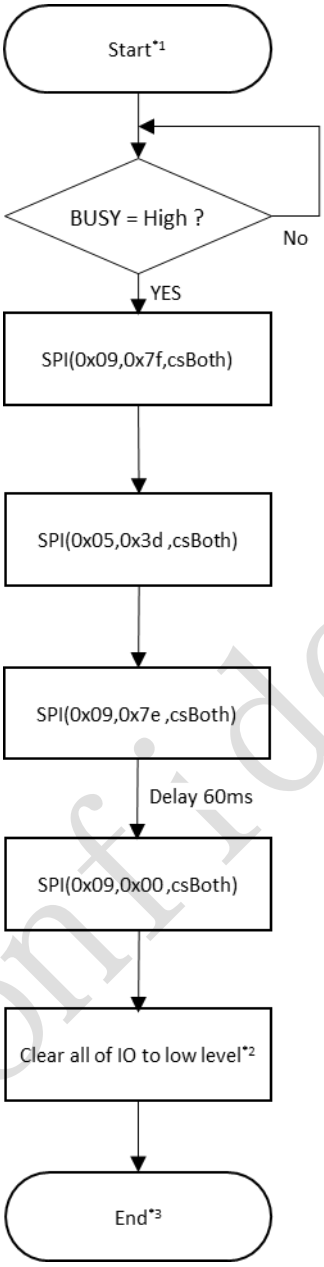


Note:

1. **Start**

   Follow the end of the COG initial flow

5 Turn-off DC/DC



Note:

1. Start

   Follow the end of the send updating command

2. VCC/VDD, RESETB, A0, CSB_M, CSB_S, SCL and SDA

3. Finished the all of the steps for update the EPD

Copyright

龍亭新技股份有限公司 Pervasive Displays Inc.

4F, No. 28, Chuangye Rd., Tainan Science Park, Tainan City 74144, Taiwan (R.O.C.)

Tel: +886-6-279-5399

http://www.pervasivedisplays.com

Revision History

Version	Date	Page (New)	Section	Description
01	2023/8/4			First official edition

Glossary of Acronyms

EPD	Electrophoretic Display (e-Paper Display)
EPD Panel	EPD
TCon	Timing Controller
FPL	Front Plane Laminate (e-Paper Film)
SPI	Serial Peripheral Interface
COG	Chip on Glass
PDI, PDi	Pervasive Displays Incorporated