Application Note

For

Small Size
Wide Temperature EPD

Description	**Interface for wide temperature EPDs. Using embedded OTP LUT supports Fast update.**
Date	**2023/10/31**
Doc. No.	
Revision	**03**

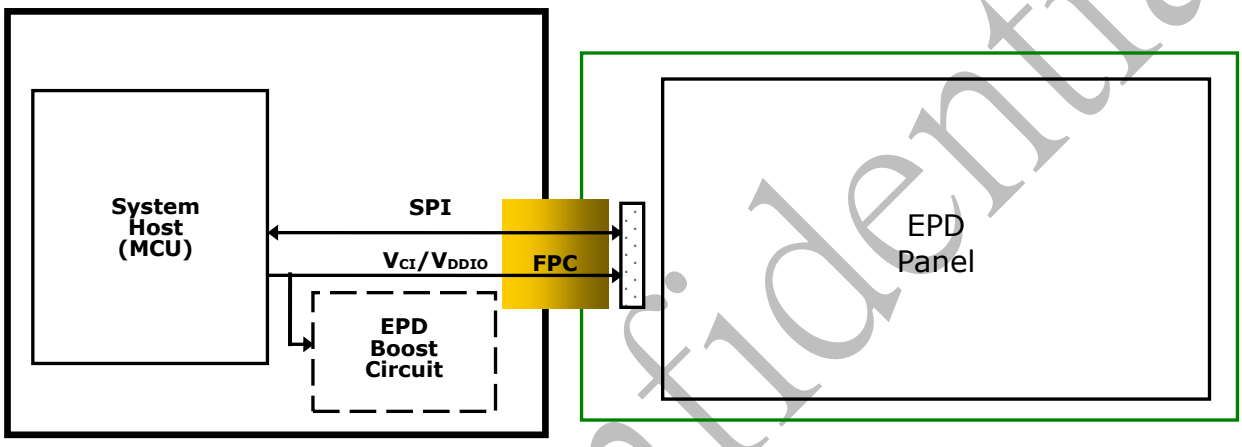
4F, No. 28, Chuangye Rd., Tainan Science Park, Tainan City 74144, Taiwan (R.O.C.)
Tel: +886-6-279-5399 Fax: +886-6-270-5857

Table of Contents

1. General Description

1.1 Overview

The document introduces how to drive the small size EPD with OTP LUT. They include the **1.54”, 2.06”, 2.13”, 2.66”, 2.7”, 2.7”(A)*1, 2.9” HR(High-resolution), 3.5” HR(High-resolution), 3.7”, 4.2” and 4.37”** wide temperature EPDs. This EPDs use single driver and that embedded T-con. The major control interface of the driver is SPI. The host sends both the setting commands and the display image to driver through the SPI bus.



Note:

1. 2.7” model name is E2271KS091, 2.7”(A) model name is E2271KS0C1, their EPD size and solution are the same.

1.2 Definition of operation mode

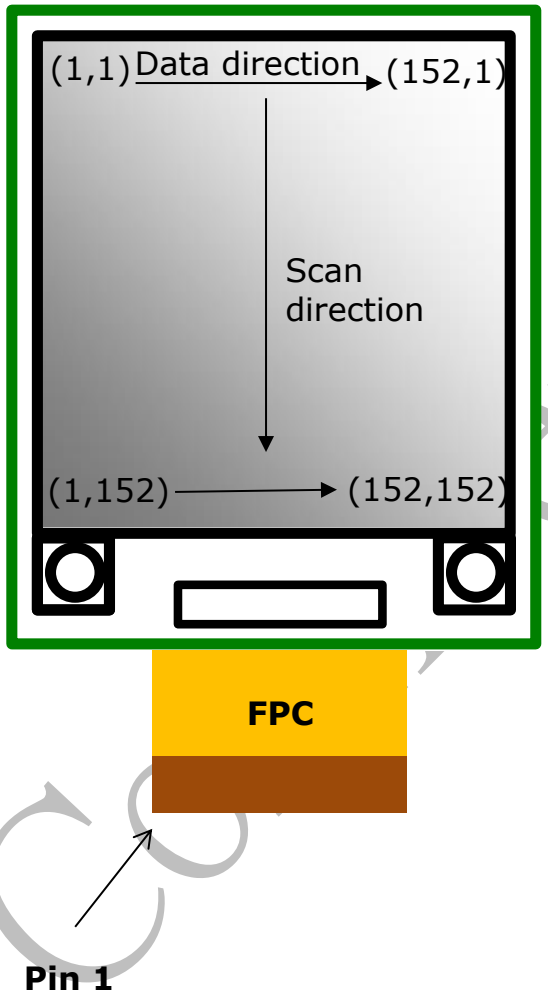
The section will define and clarify several update modes, their names are easy to confuse.

Normal update: it will perform the complete waveform for image update. The process will go through the inverse, shaking and imaging phases. The mode will take more time, but it will bring better image performance.

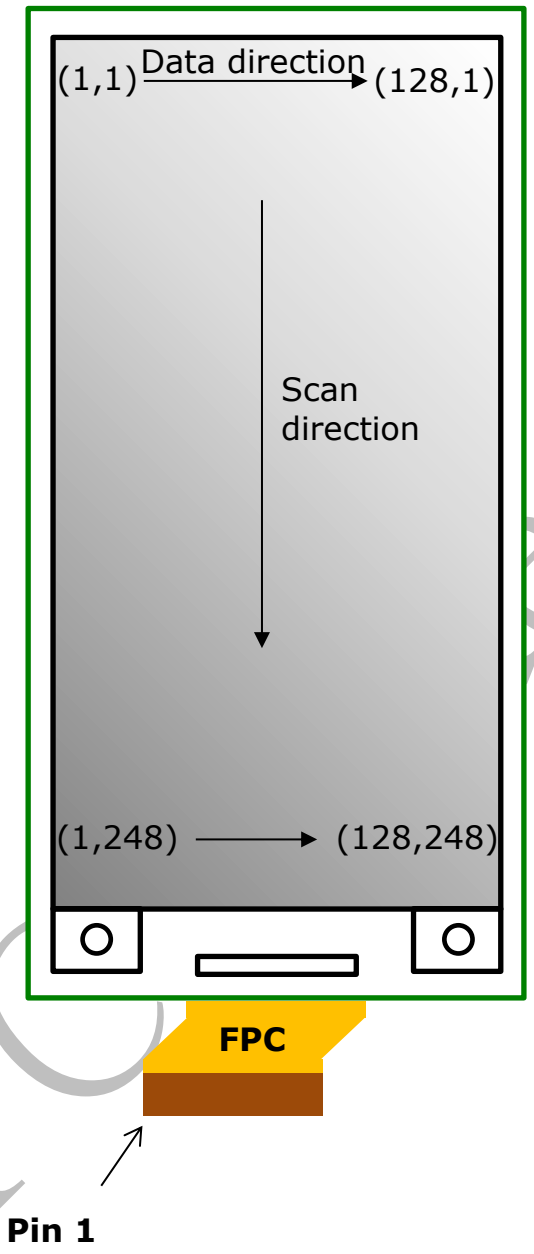
Fast update: the short waveform will be executed. COG compares the pixel data of the current image and the new image pixel by pixel, and then only drives the transition pixels. The mode can quickly complete the image update.

1.3 Panel drawing

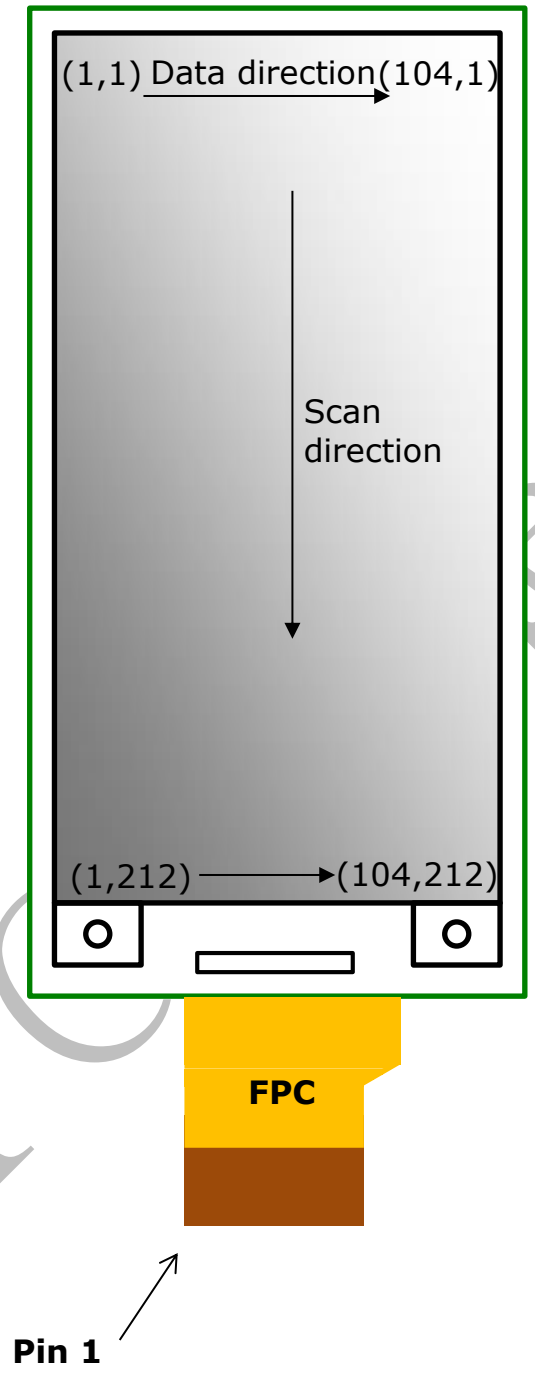
1.54-inch EPD



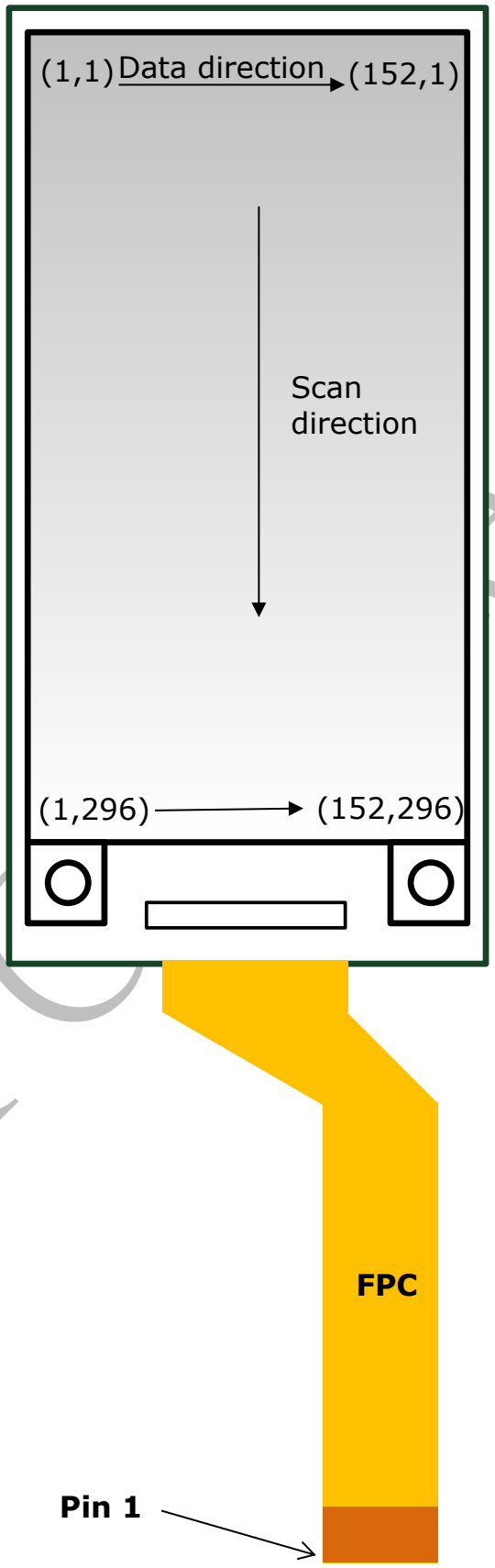
2.06-inch EPD



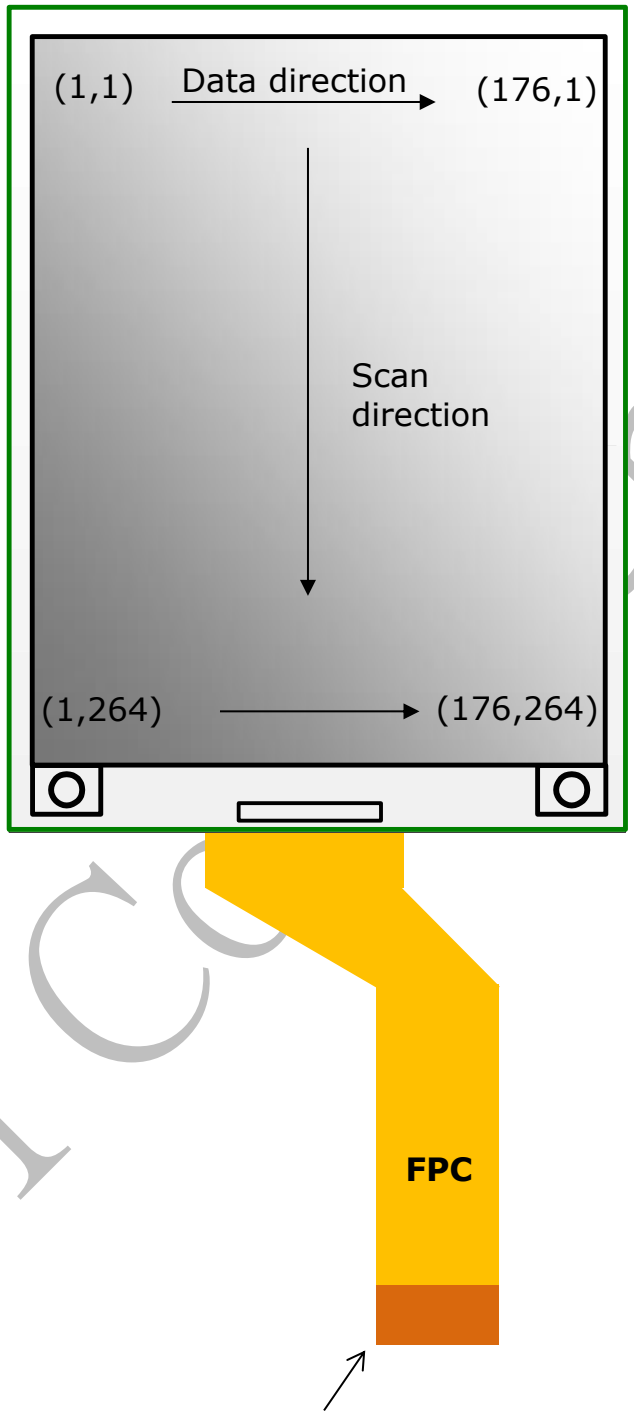
2.13-inch EPD



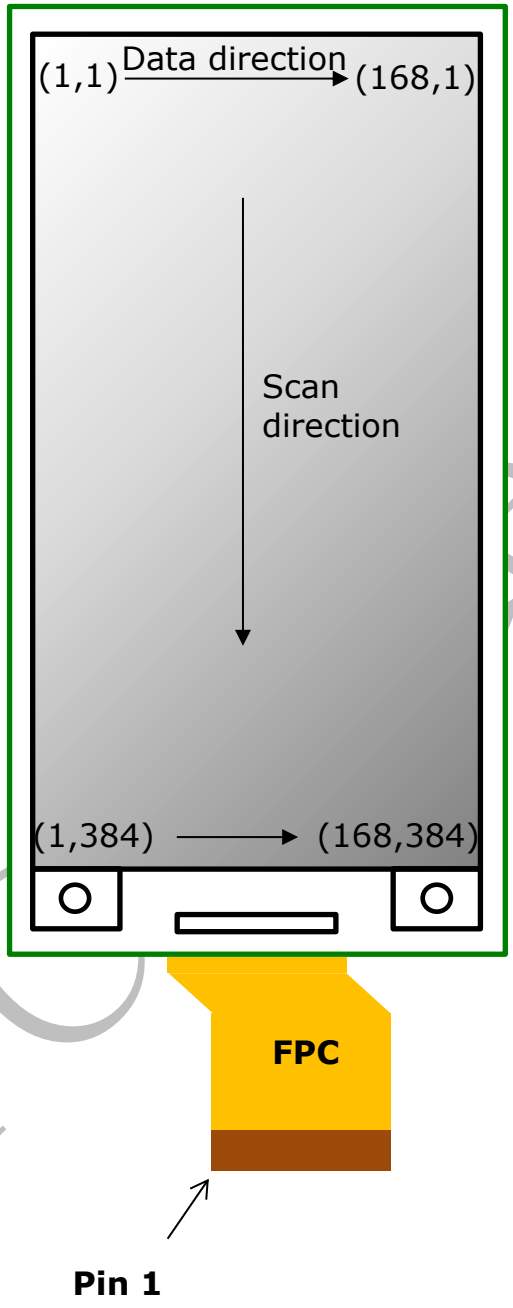
2.66-inch EPD



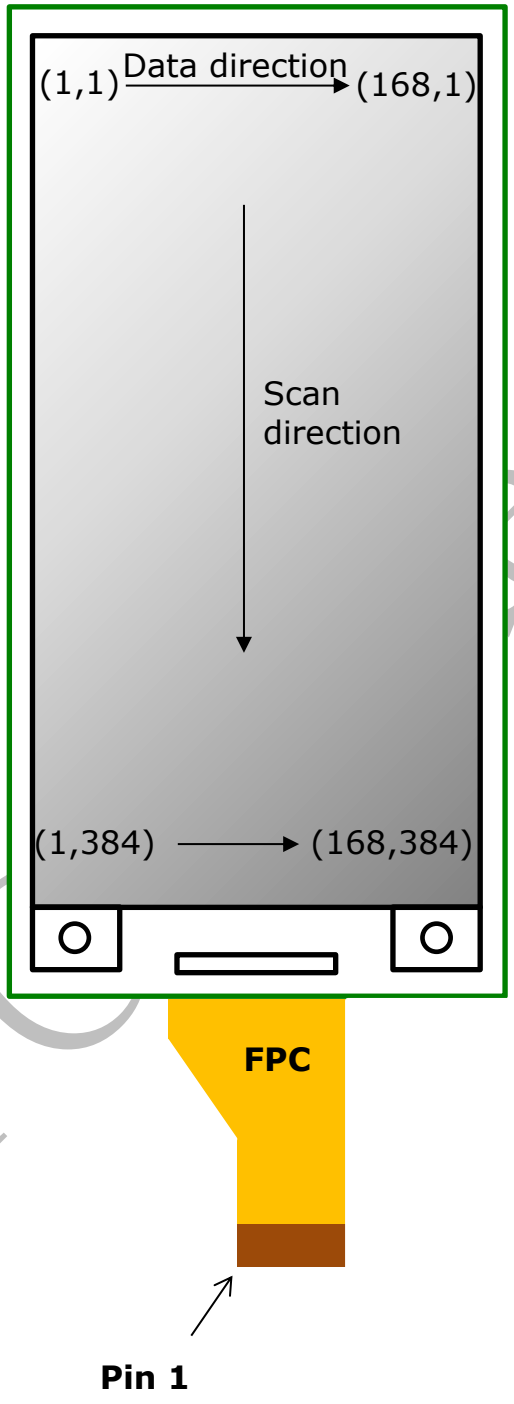
2.7-inch EPD



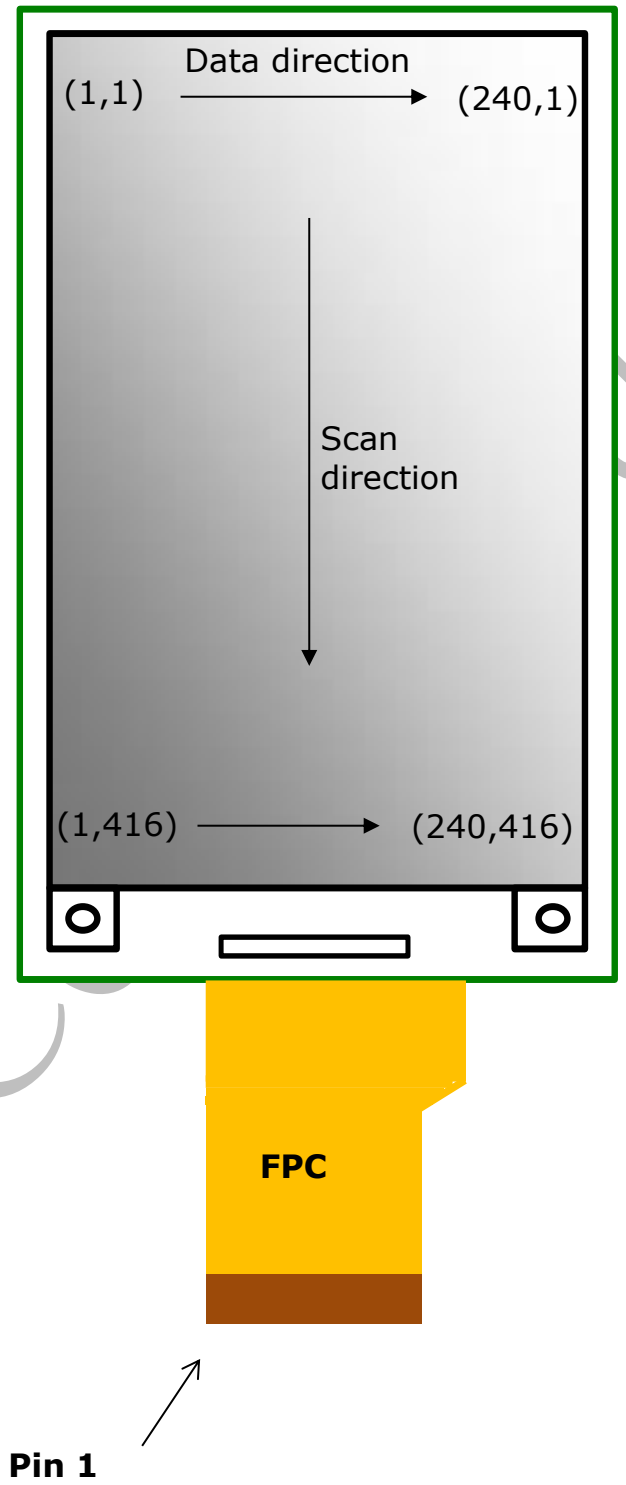
2.9-inch HR EPD



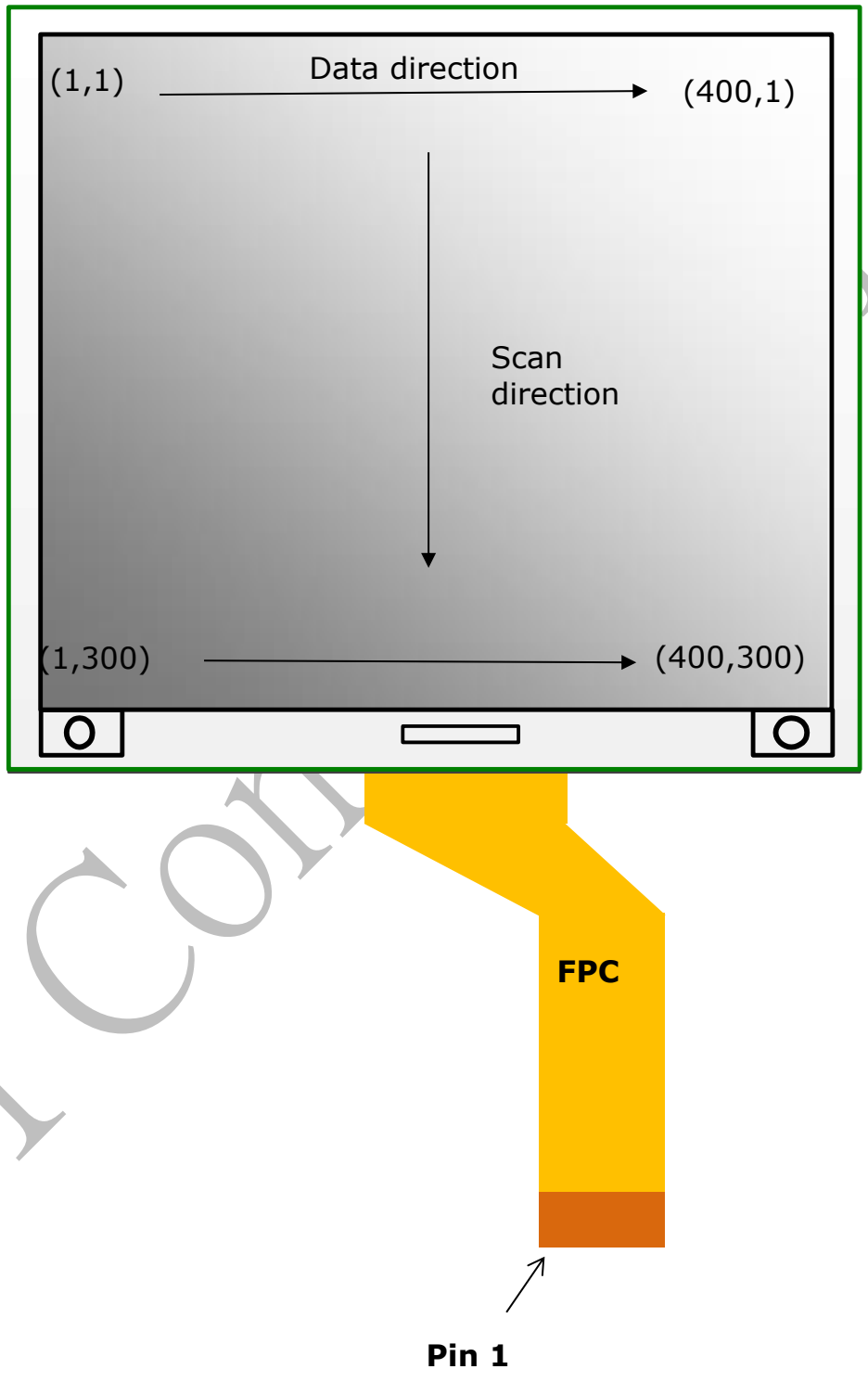
3.5-inch HR EPD



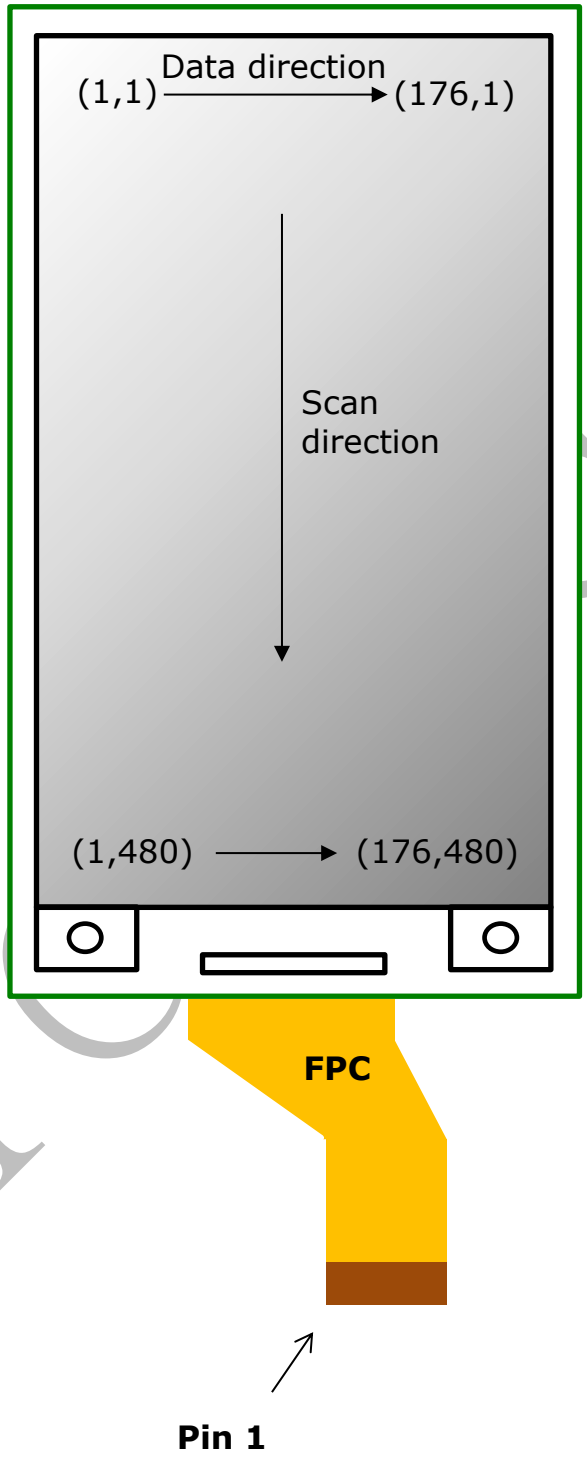
3.7-inch EPD



4.2-inch EPD

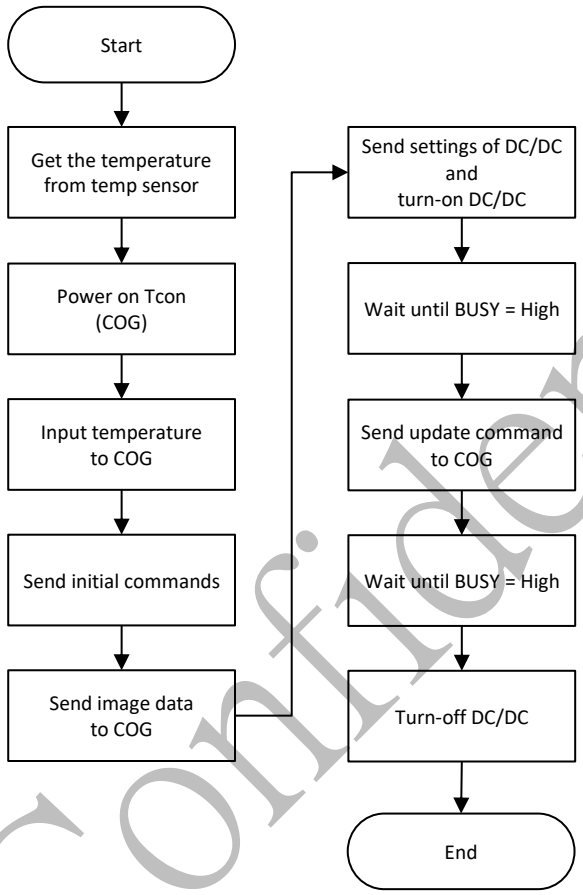


4.37-inch EPD



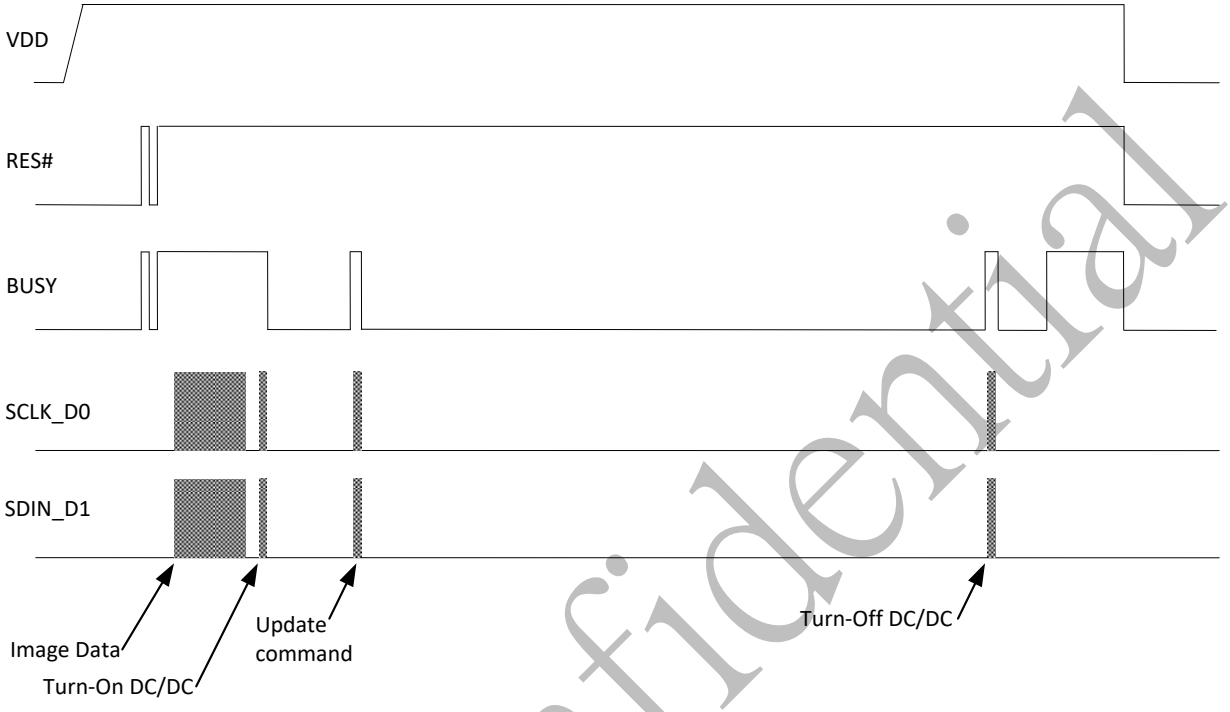
1.4 **EPD Driving Flow Chart**

The flowchart below provides an overview of the necessary actions to update the EPD. The steps below refer to the detailed descriptions in the respective sections.



1.5 **Overall Waveform**

The diagram below provides a signal control overview during an EPD update cycle.



1.6 SPI Timing Format

SPI commands are used to communicate between the MCU and the COG Driver. The SPI format used differs from the standard in that two-way communications are not used, and CS is pulled high then low between clocks. When setting up the SPI timing, PDI recommends verify both the SPI command format and SPI command timing in this section.

- SPI pin description:
  SCLK_D0 : Serial communication clock.
  SDIN_D1 : Serial communication data input/output.
  When send register index/data, the pin must be an output of MCU.
  When read data, the pin must be an input of MCU.
  D/C# : The pin is used to distinguish between register index and data.
  L : Register index. H : Data.
  CS# : Serial communication chip select.

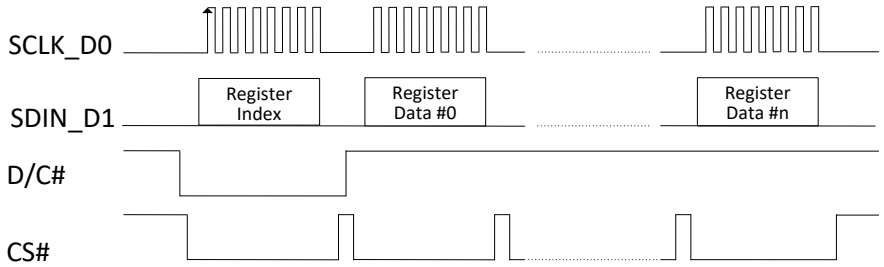
- Below is a description of the SPI Format:

  SPI(0xI, 0xD_0, 0xD_1, 0xD_2, …)

  Where:

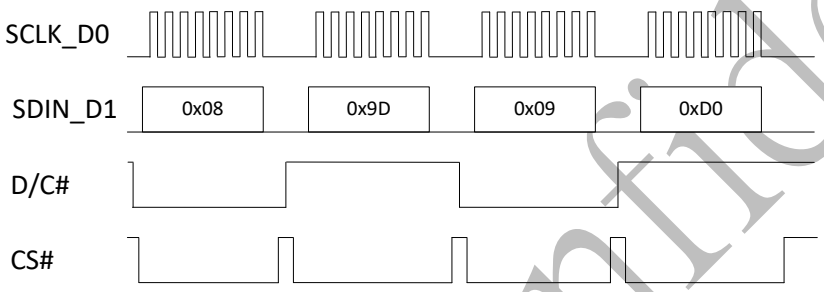
  "I" is the Register Index and the length is 1 byte
  $D_{0\sim n}$ is the Register Data. The Data length is variable by different Register Index.

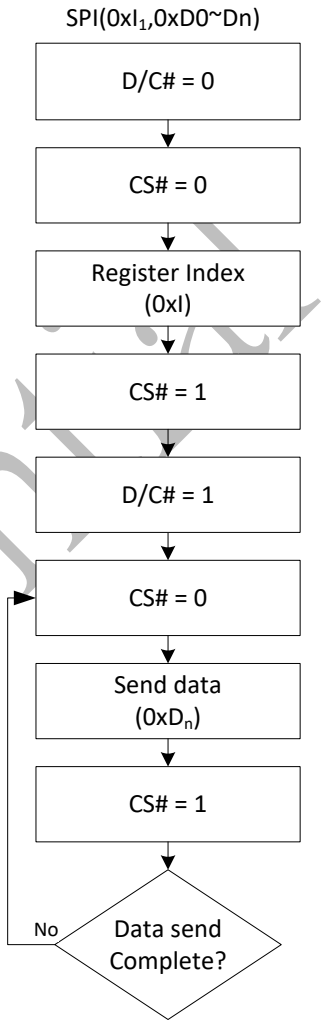
- SPI command signals and flowchart:



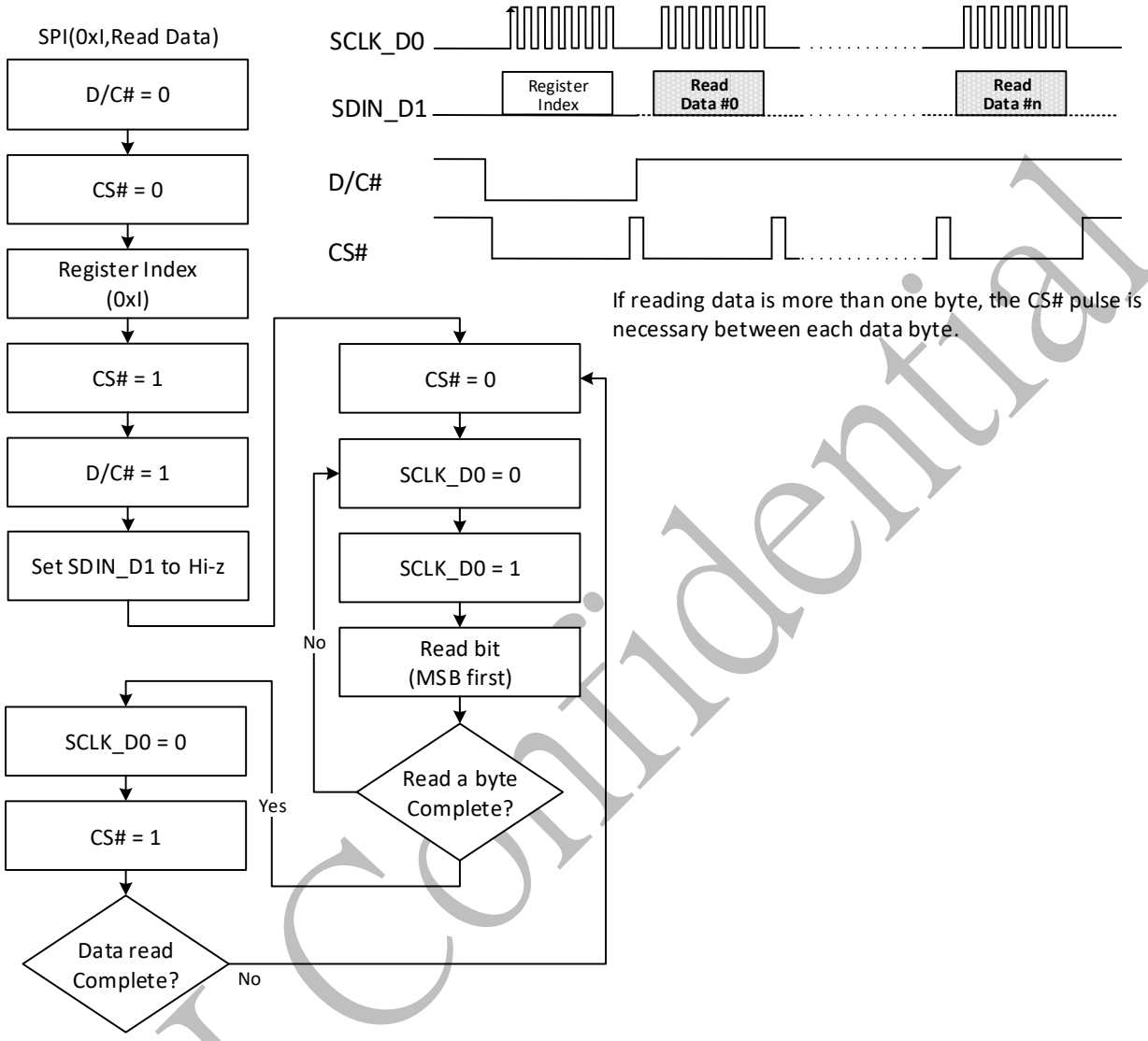
If register data is more than one byte, the CS# pulse is necessary between each data byte.

For example:
To send two SPI commands:
SPI((0x08,0x9D) and SPI(0x09, 0xD0)

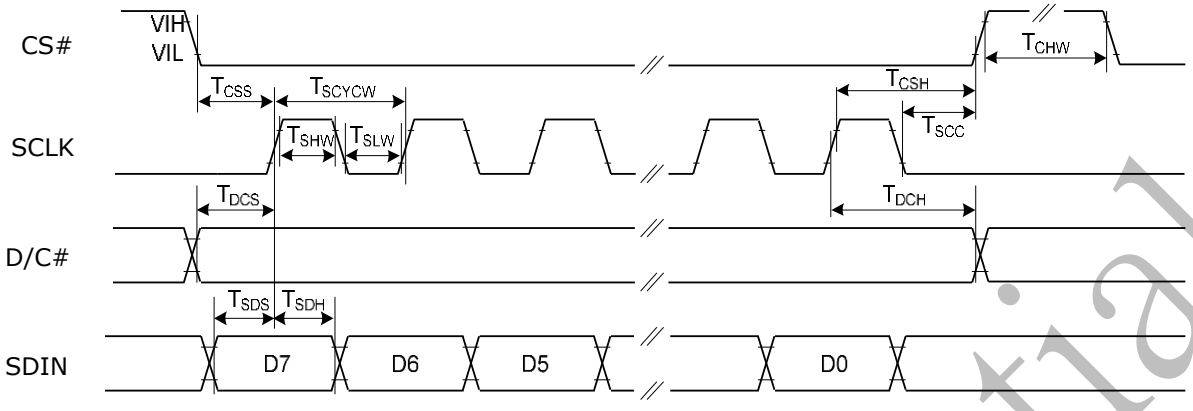




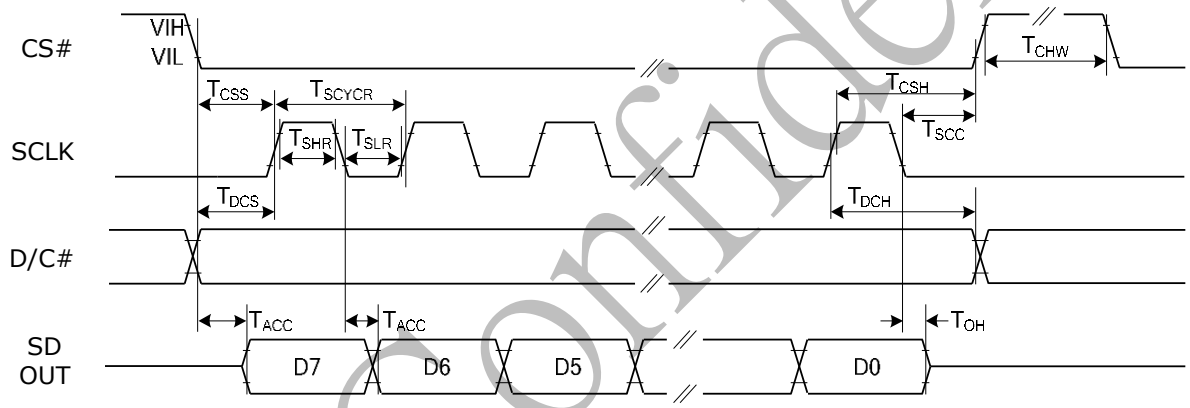
- SPI read command signals and flowchart:



- SPI command timing



Write mode



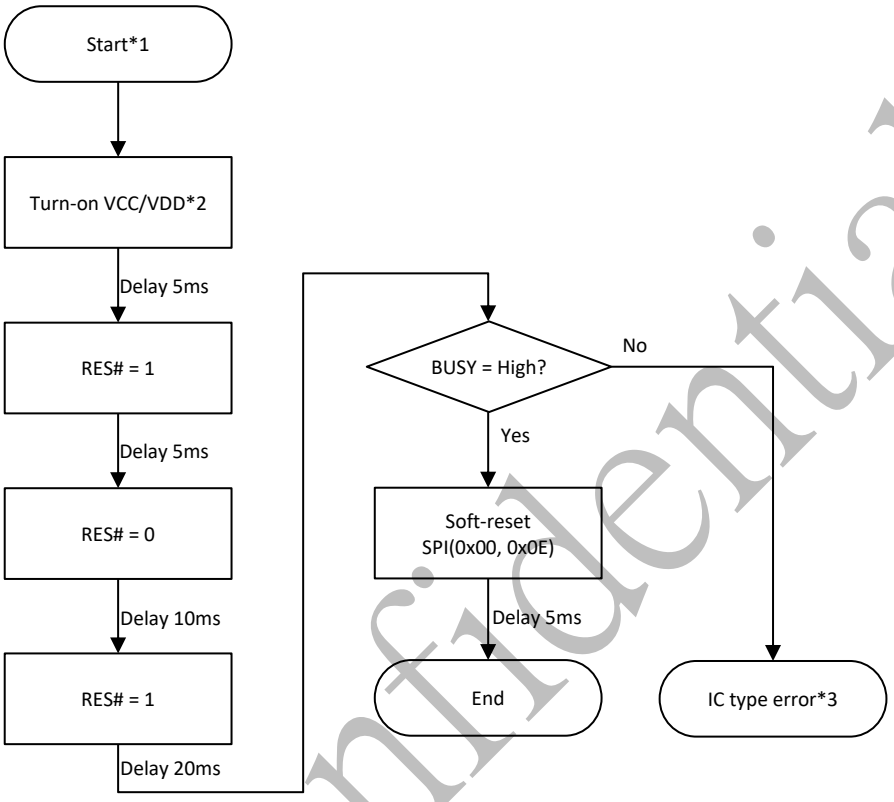
Read mode

SPI AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Chip Select Setup Time	t_{CSS}	60	-	-	ns	
Chip Select Hold Time	t_{CSH}	65	-	-	ns	
Chip Select Setup Time	t_{SCC}	20	-	-	ns	
Chip Select Setup Time	t_{CHW}	40	-	-	ns	
Serial Clock Cycle (Write)	t_{SCYCW}	100	-	-	ns	
SCLK "H" Pulse Width (Write)	t_{SHW}	35	-	-	ns	
SCLK "L" Pulse Width (Write)	t_{SLW}	35	-	-	ns	
Serial Clock Cycle (Read)						
(for 1.54", 2.66", 2.7"(A))		240	-	-		
(for 3.7", 4.2")	t_{SCYCR}	350	-	-	ns	
(for 2.06", 2.13")		270	-	-		
(for 2.7", 2.9" HR, 3.5" HR, 4.37")		150	-	-		
SCLK "H" Pulse Width (Read)						
(for 1.54", 2.66", 2.7"(A))		110	-	-		
(for 3.7", 4.2")	t_{SHR}	175	-	-	ns	
(for 2.06", 2.13")		130	-	-		
(for 2.7", 2.9" HR, 3.5" HR, 4.37")		60	-	-		
SCLK "L" Pulse Width (Read)			-	-		
(for 1.54", 2.66", 2.7"(A))		110	-	-		
(for 3.7", 4.2")	t_{SLR}	175	-	-	ns	
(for 2.06", 2.13")		130	-	-		
(for 2.7", 2.9" HR, 3.5" HR, 4.37")		60	-	-		
DC Setup Time	t_{DCS}	30	-	-	ns	
DC Hold Time	t_{DCH}	30	-	-	ns	
Data Setup Time	t_{SDS}	30	-	-	ns	
Data Hold Time	t_{DCH}	30	-	-	ns	
Access Time		-	-			
(for 1.54", 2.66", 2.7"(A))		-	-	240		
(for 3.7", 4.2")	t_{ACC}	-	-	250	ns	
(for 2.7", 2.9" HR, 3.5" HR, 4.37")		-	-	50		
(for 2.06", 2.13")		-	-	270		
Output Disable Time	t_{OH}	15	-	-	ns	

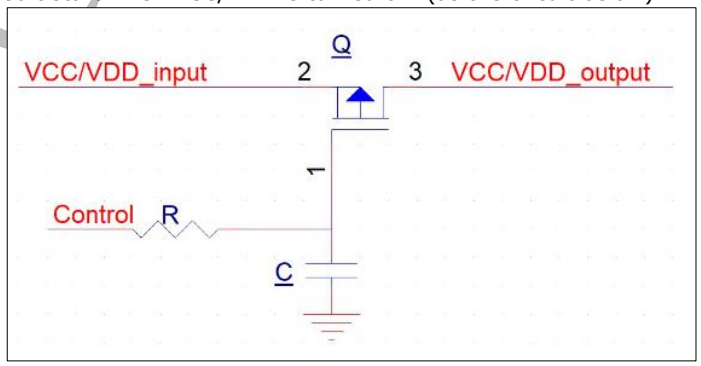
2. Power on COG driver

This flowchart describes power sequence for driver chip.



Note:

1. Start: initial state the VCC/VDD, RES#, CS#, SDIN, SCLK = 0
2. In order to the inrush current will case other issue. It is recommended to add soft start when VCC/VDD is turned on. (as the circuit below)

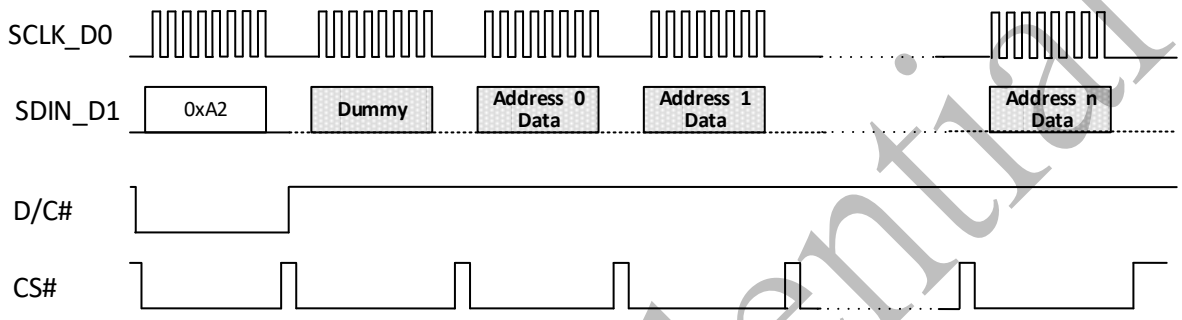


3. This document does not apply to the EPD.

3. Read OTP memory

Read OTP memory to get PSR data, PSR data must be sent in the next chapter. The OTP memory can be read by register index 0xA2, the first reading data may be dummy.

For example:
To read the OTP memory:
SPI((0xA2,Read address 0 ~ n data)



There are two bank space in OTP memory. When the data are read out, the first step is to determine which space is the active space (Bank0 orBank1).

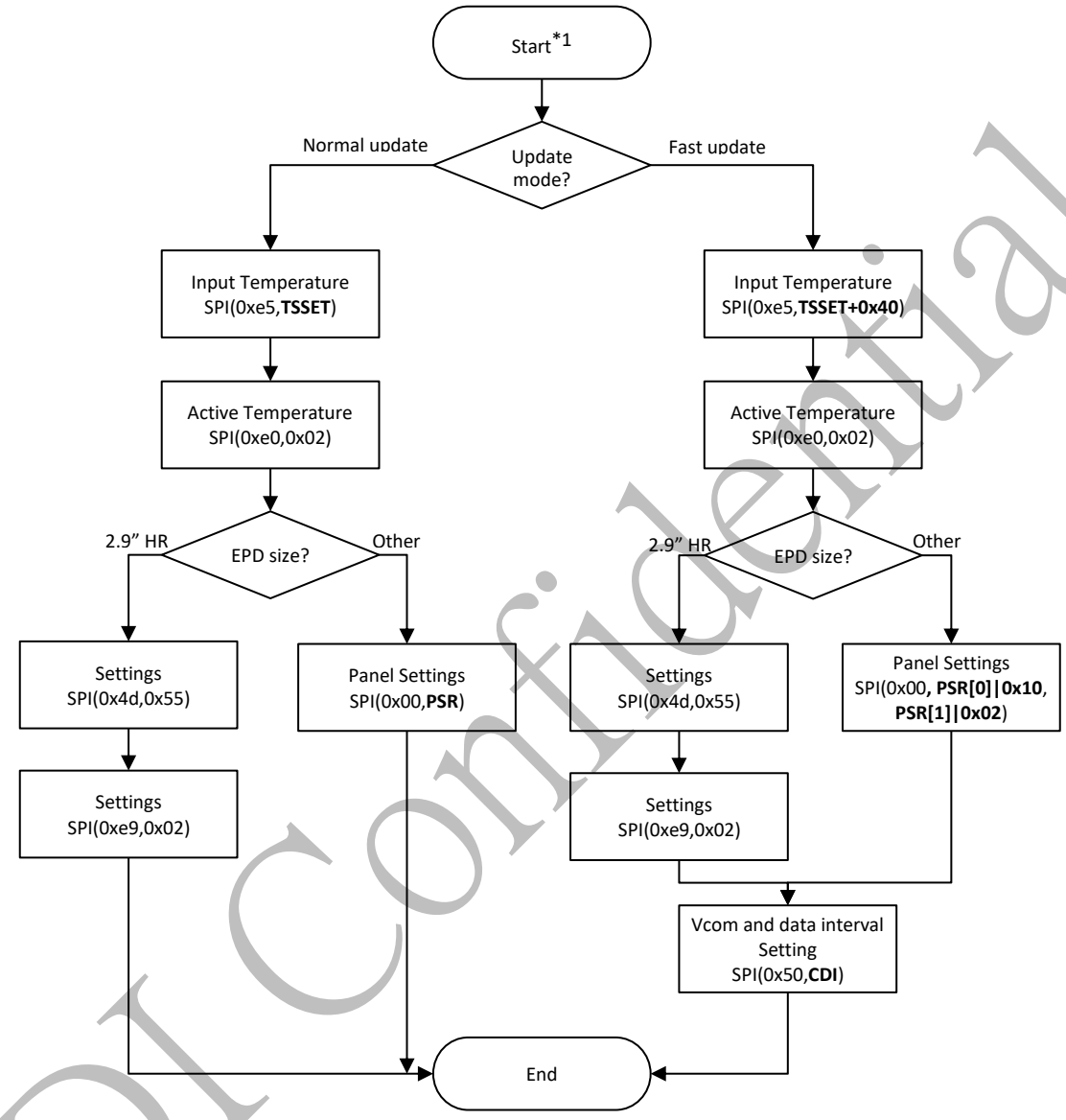
If the address 0 data is "**0xA5**", the active space is Bank0. If else the active space is Bank1.

The table indicates which address can read out the PSR data of each size EPD.

EPD Size	Active bank	PSR[0] Addr.	PSR[1] Addr.
2.7"	bank0	0x4B	0x4C
	bank1	0x4B	0x4C
1.54", 2.66", 2.7"(A), 3.5" HR, 3.7", 4.37"	bank0	0xFB4	0xFB5
	bank1	0x1FB4	0x1FB5
2.06", 2.13"	bank0	0xB1B	0xB1C
	bank1	0x171B	0x171C
4.2"	bank0	0xB1F	0xB20
	bank1	0x171F	0x1720

4. Input initial command

Please send the initial command to EPD according to the flowchart.



Note:

1. Start: Follow the end of the power on sequence.
2. **TSSET**: is the temperature value and unit are degree of Celsius. The highest bit of the data represents positive/negative in temperature.
   If it's positive, the data = (temperature value)
   If it's negative, the data = (2's complement of temperature value)
   Example:

Temperature value	data
25˚C	0x19
-5˚C	0xFB
-15˚C	0xF1

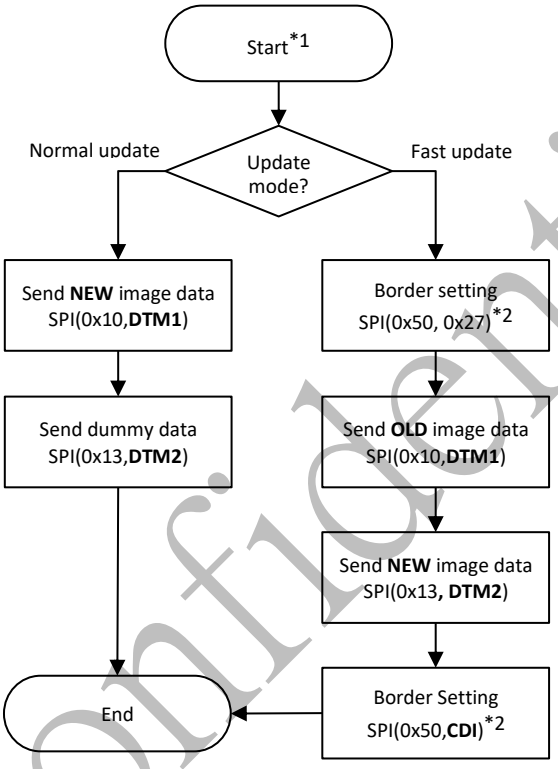
   The operate temperature range for wide temperature EPD is different between Normal and Fast update.
   Normal update : 60˚C ~ -15˚C
   Fast update : 50˚C ~ 0˚C

***** The TSSET cannot be set outside of this range. *****
***** Otherwise, the EPD will be update abnormal. *****

3. **CDI**: this is a constant value of 0x07.
4. **PSR**: should be read out from OTP. Please refer to chapter 3 to see how to get this data.

5. Input image to the EPD

This section describes how to send the image data into the COG driver. EPD needs to receive two frames image data each update but the image data definitions of "Normal" update and "Fast" update are different. The two frames image data must be sent into EPD from register of **0x10** and **0x13** respectively.



Note:

1. Start: Follow the end of the initial command.
2. Border Setting: this command is only for 1.54", 2.06", 2.13", 2.66", 2.7"(A), 3.5" HR, 3.7" and 4.37".
   2.7", 2.9" HR and 4.2" don't need to send this command. **CDI** is a constant value of 0x07.

5.1 DTM1, DTM2 Definition

DTM1 and DTM2 mean the image data of the first frame and the second frame, respectively. Their definitions are different between "Normal update" and "Fast update".

DTM1:

For Normal update, it is the NEW image data that you want displaying next moment.

For Fast update, it is the OLD image data that already displayed on the EPD.

DTM2:

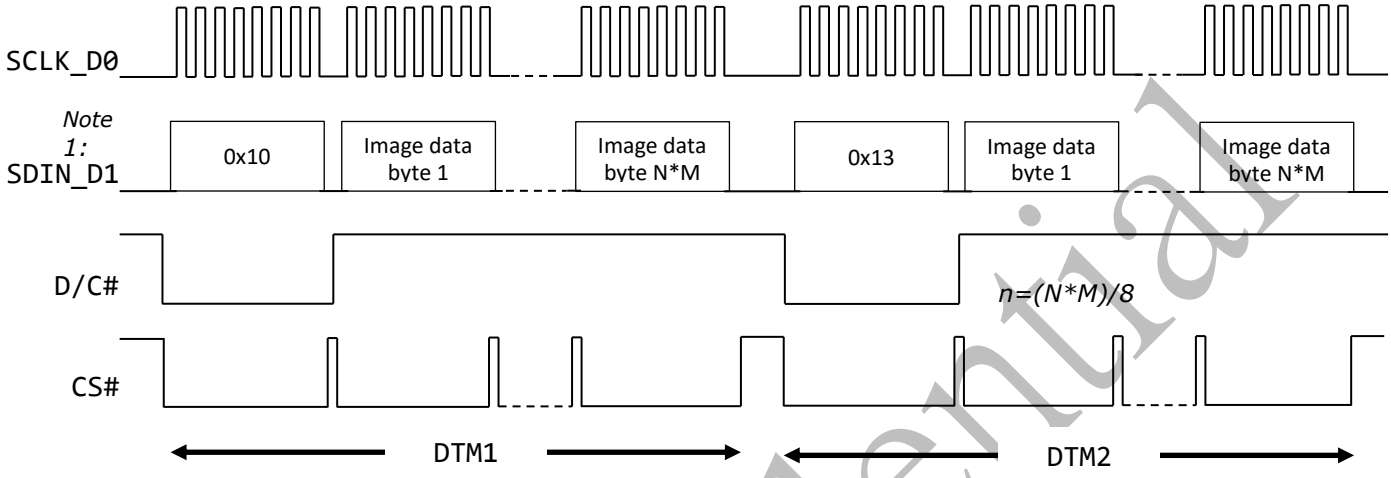
For Normal update, it is dummy data. It just needs to be filled with the enough amount of 0x00.

For Fast update, it is the NEW image data that you want displaying next moment.

Data	Pixel Color
1	Black
0	White

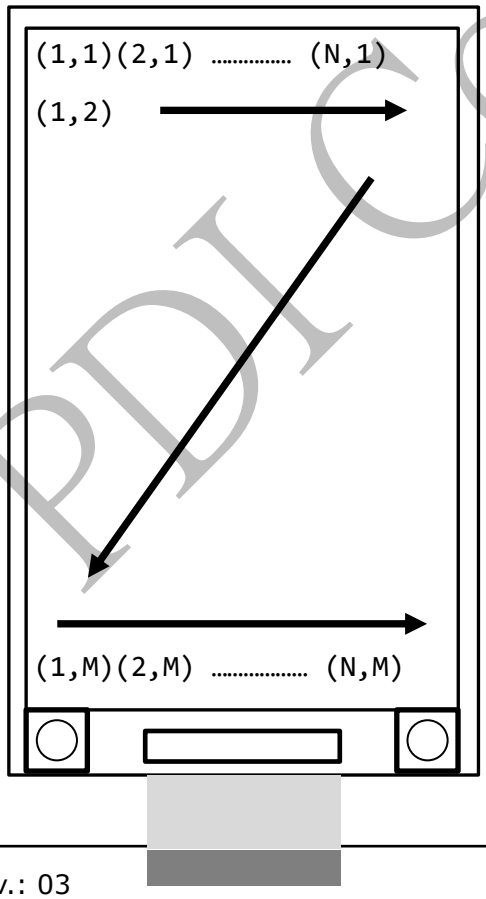
5.2 Image data sending (DTM1, DTM2)

This section describes how to send the DTM1 and DTM2 data and how mapping to real pixel. User needs to send enough image data into COG through both register 0x10(DTM1) and 0x13(DTM2).



The data of image frame, one bit represents 1 pixel. (e.g. the first byte represents the 1st ~ 8th pixels of the first line, the second byte represents the 9th ~ 16th pixels of the first line, …… and so on).

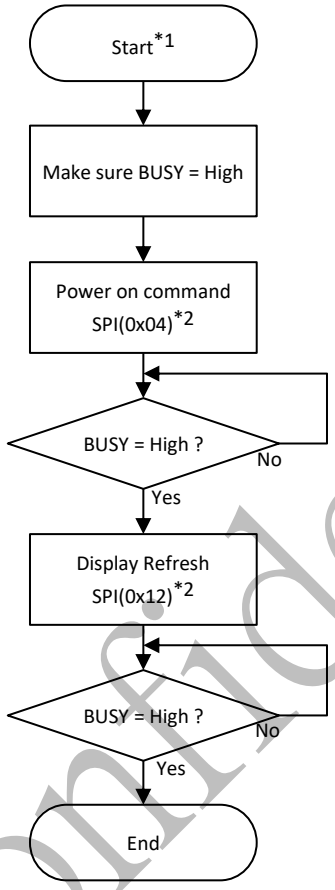
Data Byte	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Pixel	P[n]	P[n+1]	P[n+2]	P[n+3]	P[n+4]	P[n+5]	P[n+6]	P[n+7]




```
Image data input sequence:
Line001:(1,1)>(2,1)>…>(N,1)
Line002:(1,2)>(2,2)>…>(N,2)
                :
                :
                :
Line  M:.............(N,M)
A Frame Total : 1 x N x M bits
           = (N x M)/8 Bytes
```

EPD size	N	M	Total bytes/frame
1.54”	152	152	2,888
2.06”	128	248	3,968
2.13”	104	212	2,756
2.66”	152	296	5,624
2.7”	176	264	5,808
2.9” HR	168	384	8,064
3.5” HR	232	480	13,920
3.7”	240	416	12,480
4.2”	400	300	15,000
4.37”	176	480	10,560

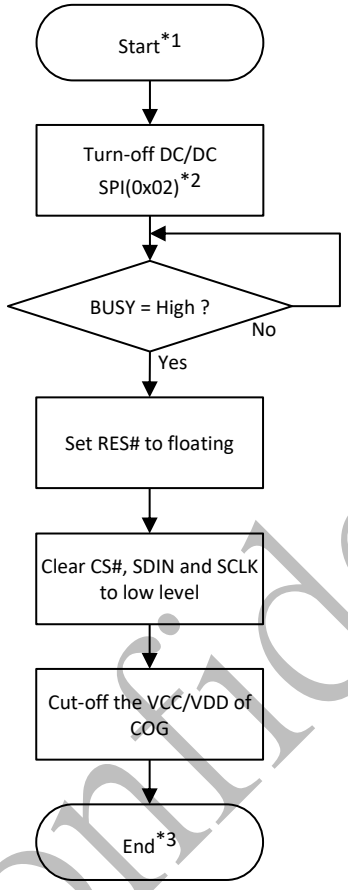
6. Send updating command



Note:

1. Start: Follow the end of the input image sequence
2. This register does not have data, just need send the index

7. Turn-off DC/DC



Note:

1. Start: Follow the end of the send updating command sequence
2. This register does not have data, just need send the index
3. Finished the all of the steps for update the EPD

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4F, No. 28, Chuangye Rd., Tainan Science Park, Tainan City 74144, Taiwan (R.O.C.)

Tel: +886-6-279-5399

http://www.pervasivedisplays.com

Revision History

Version	Date	Page (New)	Section	Description
01	2022/12/29			First issue
02	2023/09/26			New 2.9” HR EPD and update power sequence
03	2023/10/31			New 2.06”, 2.7”(A), 3.5” HR, 4.37” EPD and update 2.13” SPI timing

Glossary of Acronyms

EPD	Electrophoretic Display (e-Paper Display)
EPD Panel	EPD
TCon	Timing Controller
FPL	Front Plane Laminate (e-Paper Film)
SPI	Serial Peripheral Interface
COG	Chip on Glass
PDI, PDi	Pervasive Displays Incorporated