Application Note

for

Spectra 4 Small Size EPDs

Description	**Interface for Spectra 4 Small Size EPDs**
Date	**2023/5/22**
Doc. No.	
Revision	**01**

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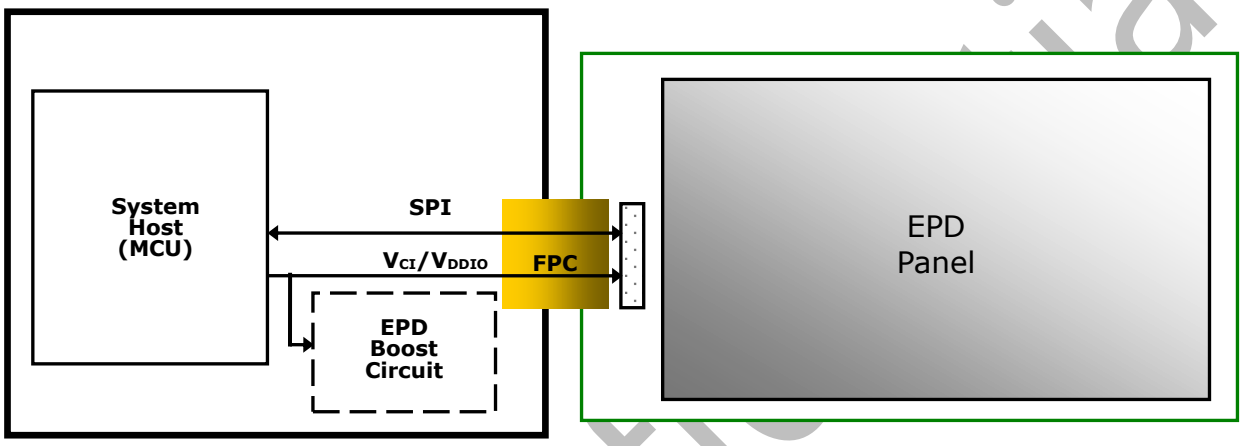
1. General Description

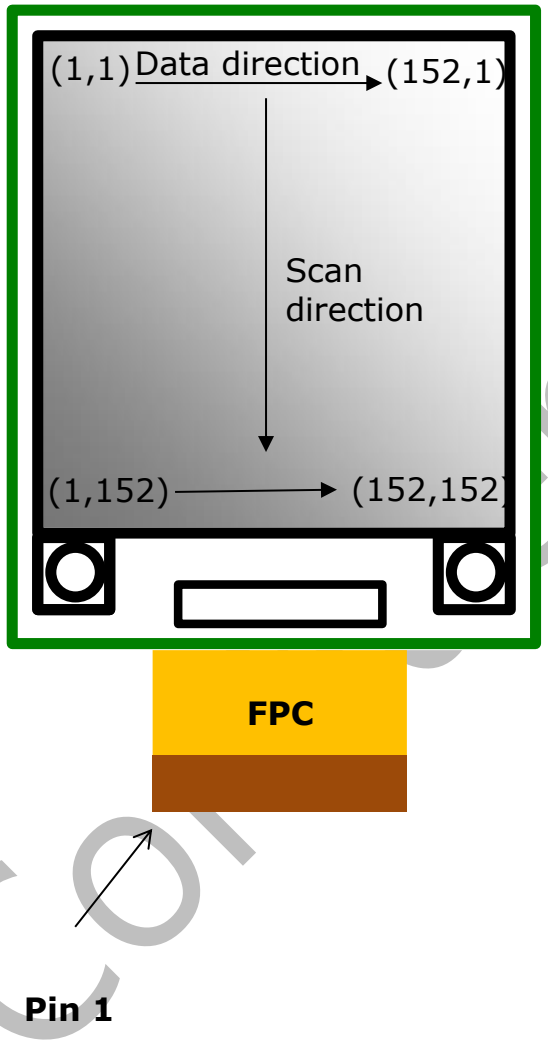
1.1 Overview

The document introduces how to drive the Spectra 4 small size EPDs with OTP LUT. They include the **1.54", 2.13" and 2.66"** EPDs. The EPDs use a single driver and that embedded T-con. The major control interface of the driver is SPI. The host sends both the setting commands and the display image to driver through the SPI bus.

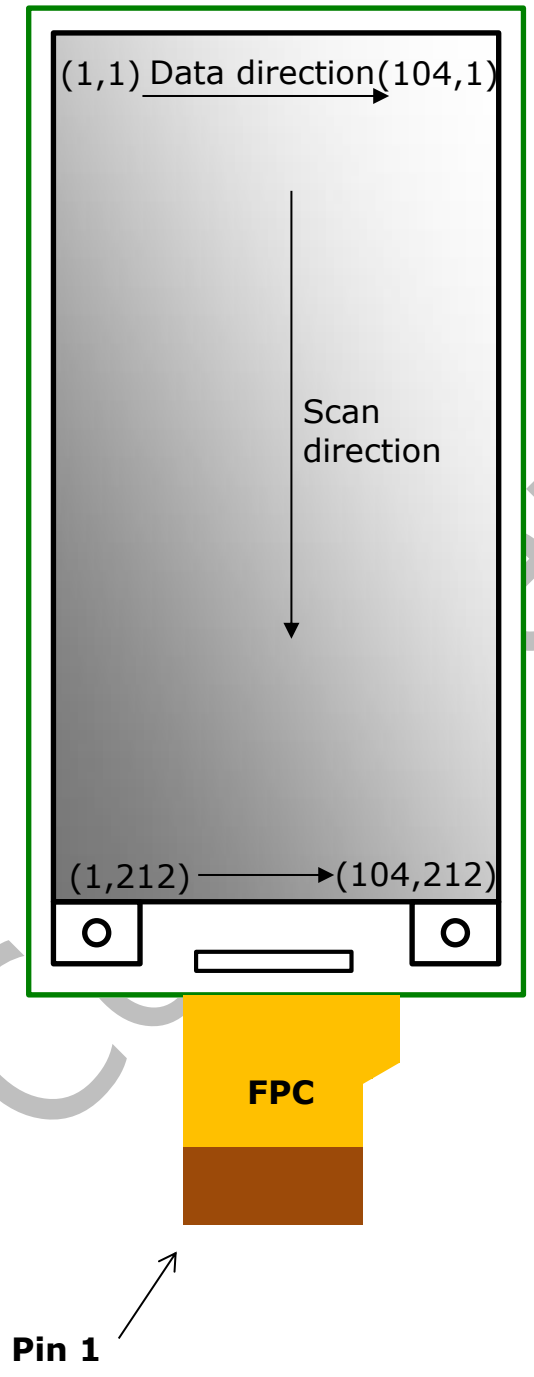


1.2 Panel drawing

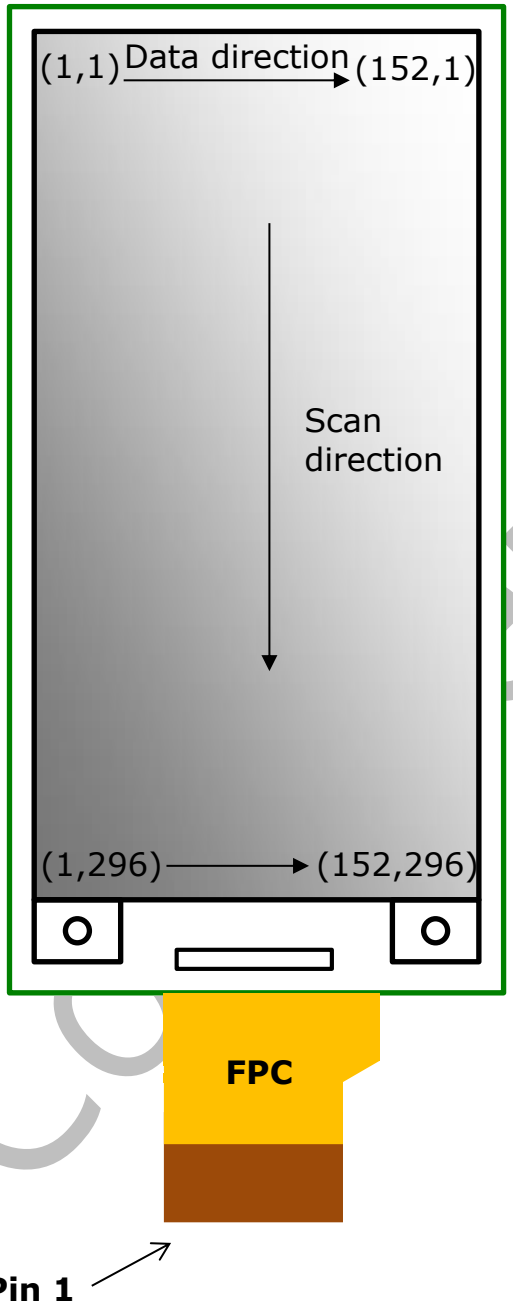
1.54-inch EPD



2.13-inch EPD

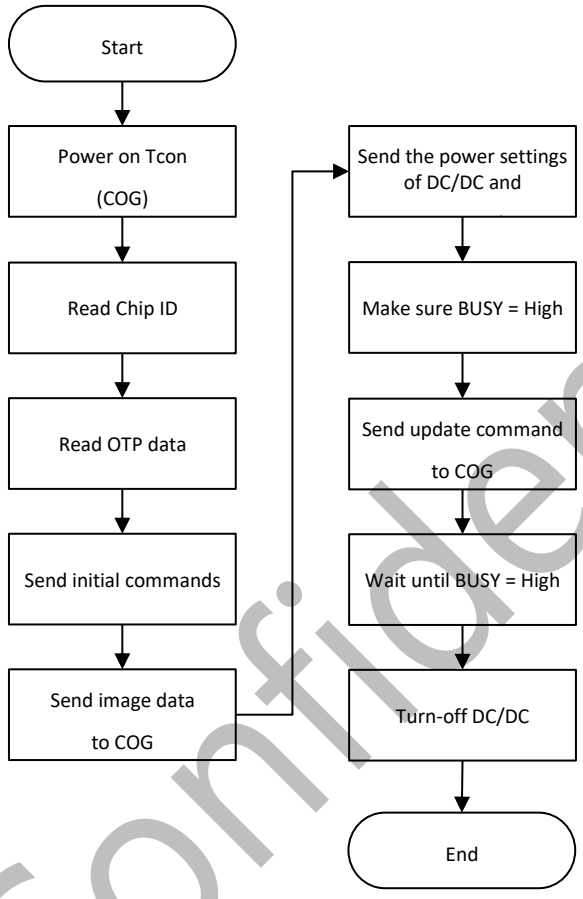


2.66-inch EPD



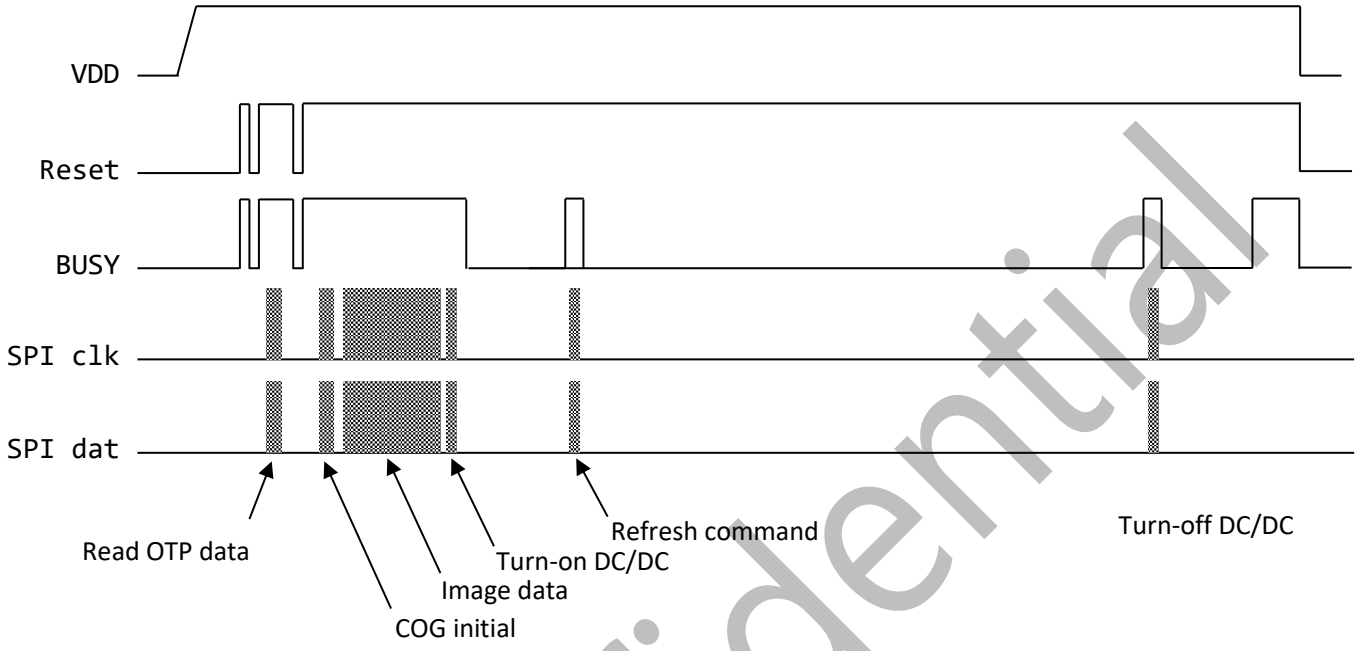
1.3 EPD Driving Flow Chart

The flowchart below provides an overview of the necessary actions to update the EPD. The steps below refer to the detailed descriptions in the respective sections.



1.4 **Overall Waveform**

The diagram below provides a signal control overview during an EPD update cycle.



1.5 SPI Timing Format

SPI commands are used to communicate between the MCU and the COG Driver. The SPI format used differs from the standard in that two-way communications are not used, and CS is pulled high then low between clocks. When setting up the SPI timing, PDI recommends verify both the SPI command format and SPI command timing in this section.

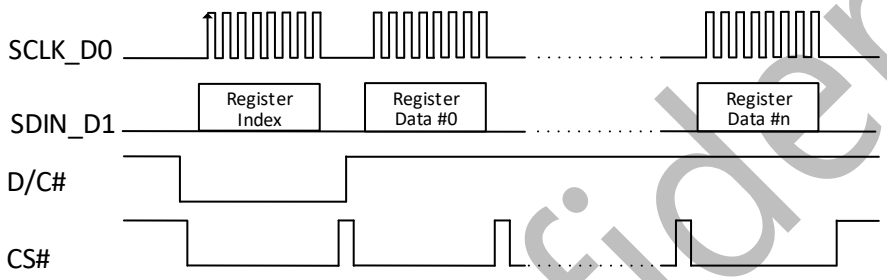
- Below is a description of the SPI Format:

  SPI(0xI, 0xD_0, 0xD_1, 0xD_2, …)

  Where:

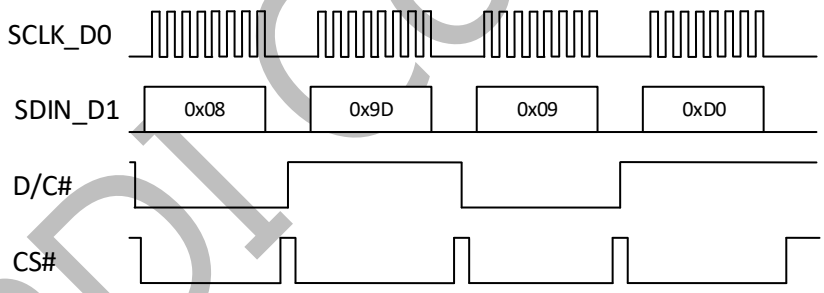
  I is the Register Index and the length is 1 byte
  $D_{0\sim n}$ is the Register Data or the Reading Data. The Data length is variable by different Register Index.

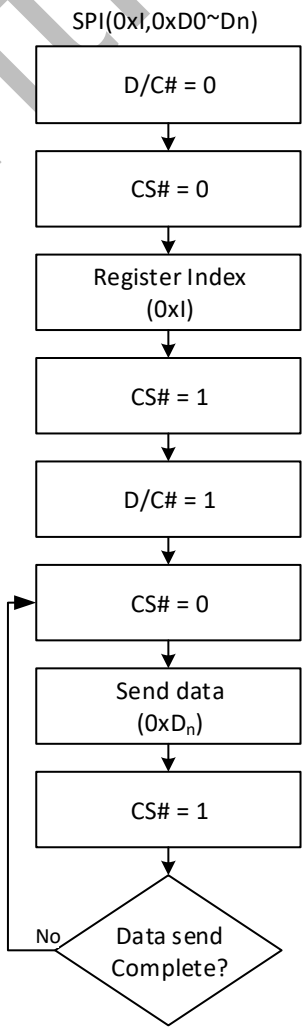
- SPI send command signals and flowchart:



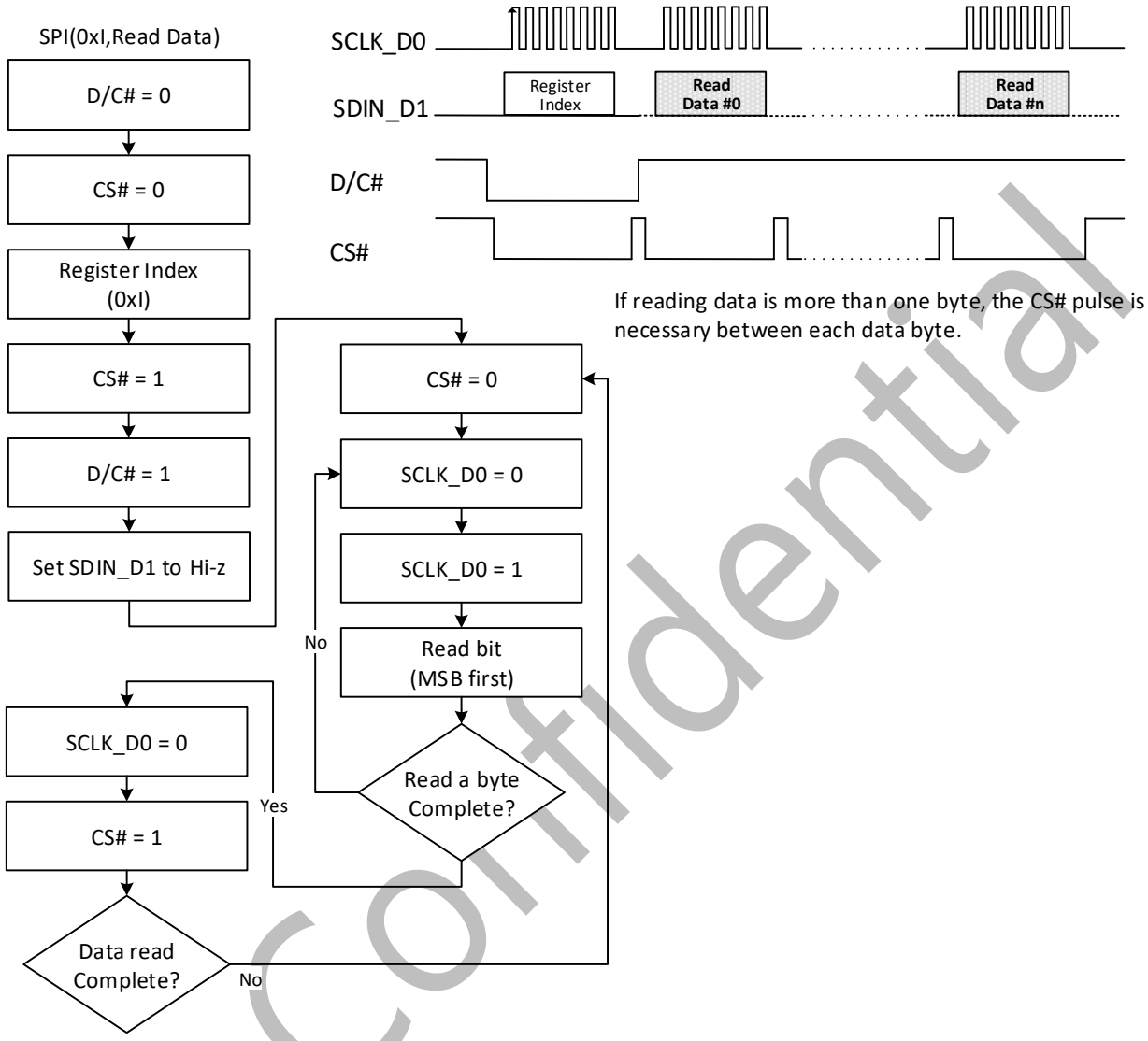
If register data is more than one byte, the CS# pulse is necessary between each data byte.

For example:
To send two SPI commands:
SPI((0x08,0x9D) and SPI(0x09, 0xD0)

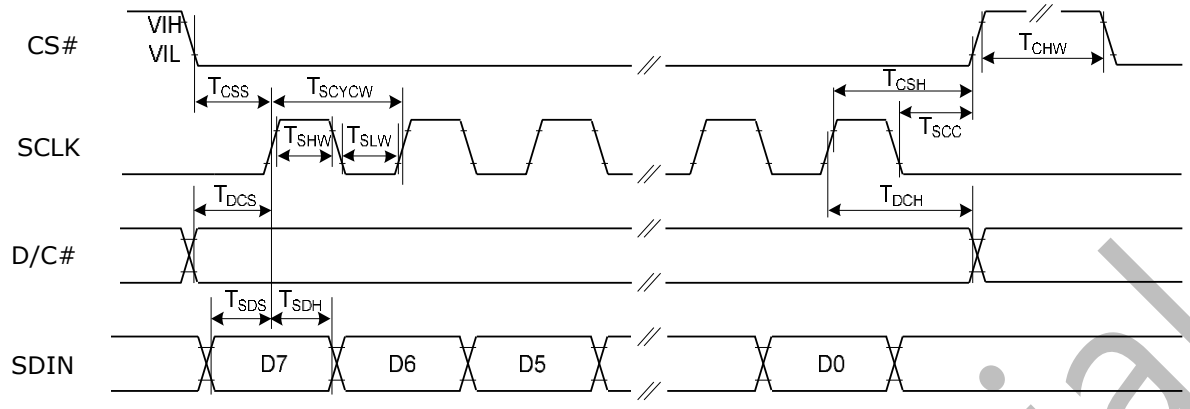




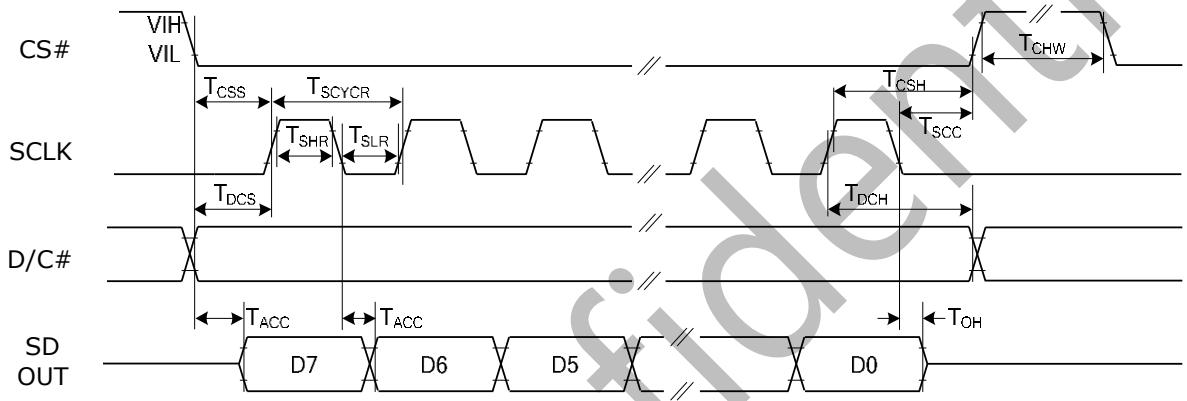
- SPI read command signals and flowchart:



- SPI command timing



Write mode



Read mode

AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Chip Select Setup Time	t_{CSS}	60	-	-	ns	
Chip Select Hold Time	t_{CSH}	65	-	-	ns	
Chip Select Setup Time	t_{SCC}	20	-	-	ns	
Chip Select Setup Time	t_{CHW}	40	-	-	ns	
Serial Clock Cycle (Write)	t_{SCYCW}	100	-	-	ns	
SCLK "H" Pulse Width (Write)	t_{SHW}	35	-	-	ns	
SCLK "L" Pulse Width (Write)	t_{SLW}	35	-	-	ns	
Serial Clock Cycle (Read)	t_{SCYCR}	150	-	-	ns	
SCLK "H" Pulse Width (Read)	t_{SHR}	60	-	-	ns	
SCLK "L" Pulse Width (Read)	t_{SLR}	60	-	-	ns	
DC Setup Time	t_{DCS}	60	-	-	ns	
DC Hold Time	t_{DCH}	65	-	-	ns	
Data Setup Time	t_{SDS}	30	-	-	ns	
Data Hold Time	t_{SDH}	30	-	-	ns	
Access Time	t_{ACC}	-	-	50	ns	
Output Disable Time	t_{OH}	15	-	-	ns	

1.6 **Read OTP memory mapping data**

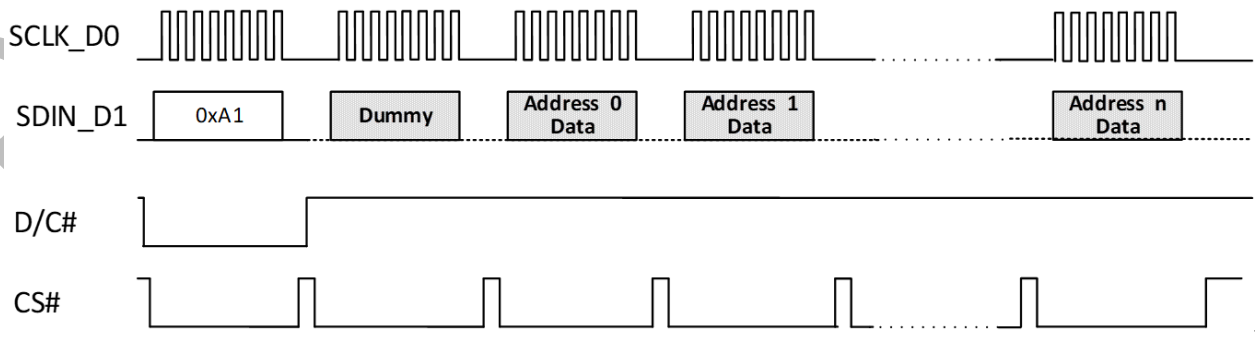
There are two sectors of memory in OTP that were programmed the User-defined data and COG initial data. This paragraph is going to describe how to read out these data.

For 1.54", 2.13" and 2.66"

	ADDRESS	DATA	DESCRIPTION
OTP memory	0x0000 | 0x14FF	Eink Reserves	
	0x1500	check code	Check code means whether the OTP data is valid. It should be 0xA5.
	0x1501	Layout Rev	This unique version-number identifies the memory layout.
	0x1502	COG TYPE	COG ID
	0x1503	Vendor	Vendor ID
	0x1504	Waveform Rev	Revision of the waveform
	0x1505 | 0x150A	FPL lot name	The 6-byte means the FPL lot name, it is 6-character ASCII encoding. For example, FPL-lot "SMM069" will be written as 0x53,0x4D,0x4D,0x30,0x36,0x39
	0x150B	Color	The colors supported by this EPD 0x04 -> It supports black/white/red/yellow
	0x150C | 0x150F	Eink Reserves	
	0x1510 | 0x152F	COG initial data	The data of this sector are the necessary IC initial data. These data need to be read out for IC initialization.
	0x1530 | ……	Eink Reserves	

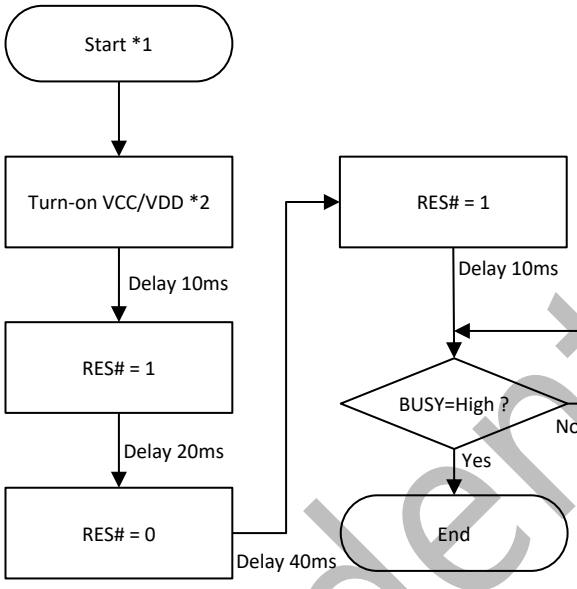
The OTP memory can be read by register index 0xA1, the first reading data is dummy.

For example:
To read the OTP memory:
SPI((0xA1,Read address 0 ~ n data)



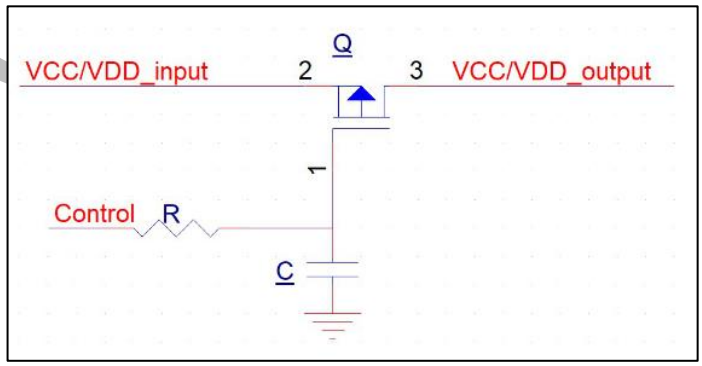
2. Power on COG driver

This flowchart describes power sequence for driver chip.

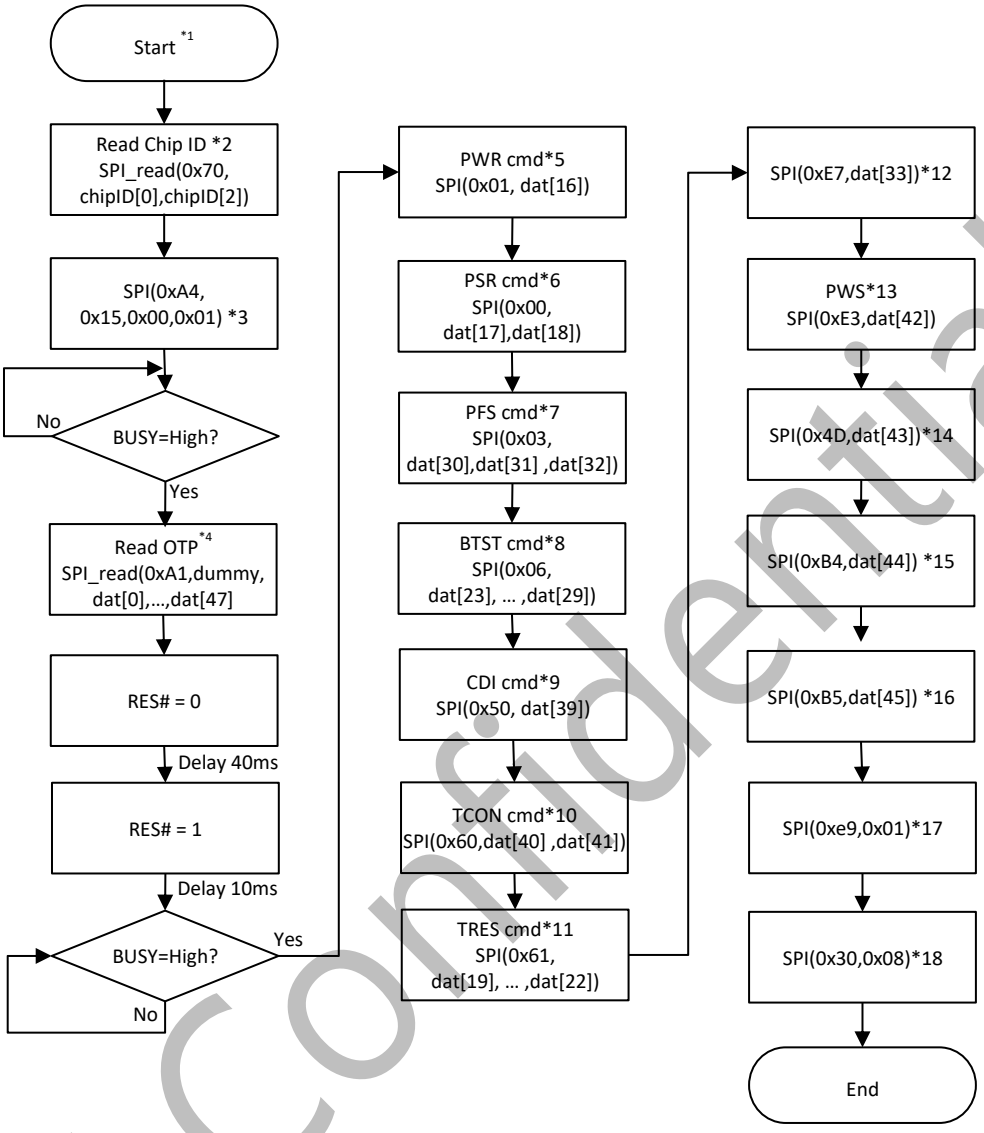


Note:

1. Start: initial state the VCC/VDD, RES#, CS#, SDIN, SCLK, BS, D/C = 0
2. In order to the inrush current will case other issue. It is recommended to add soft-start when VCC/VDD is turned on. (as the circuit below)



3. COG initial



NOTE:

1. Start: Follow the end of the power on sequence
2. Chip ID: Chip ID of E2806 would be {0x03,0x02}
3. This command is referred to Eink's sample code. It should be applied for assigning the beginning address of OTP reading.
4. Read OTP: the first byte of read out is dummy byte. According to the OTP mapping table, the necessary data is from 0x1500 ~ 0x152F, so there are 48 bytes data that need to be read out and store these data into the "**dat**" array.
5. PWR: this is 1-byte data read from **0x1510** of OTP memory, which is equivalent to **dat[16]**
6. PSR: this is 2-byte data read from **0x1511~0x1512** of OTP memory, which is equivalent to **dat[17~18]**
7. PFS: this is 2-byte data read from **0x151E~0x1520** of OTP memory, which is equivalent to **dat[30~32]**
8. BTST: this is 7-byte data read from **0x1517~0x151D** of OTP memory, which is equivalent to **dat[23~29]**
9. CDI: this is 1-byte data read from **0x1527** of OTP memory, which is equivalent to **dat[39]**
10. TCON: this is 2-byte data read from **0x1528~0x1529** of OTP memory, which is equivalent to **dat[40~41]**
11. TRES: this is 4-byte data read from **0x1513~0x1516** of OTP memory, which is equivalent to **dat[19~22]**

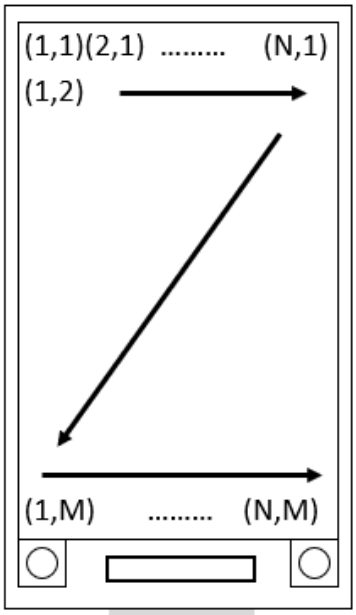
12. The 0xE7 setting is 1-byte data read from **0x1521** of OTP memory, which is equivalent to **dat[33]**
13. PWS: this is 1-byte data read from **0x152A** of OTP memory, which is equivalent to **dat[42]**
14. The 0x4D setting is 1-byte data read from **0x152B** of OTP memory, which is equivalent to **dat[43]**
15. The 0xB4 setting is 1-byte data read from **0x152C** of OTP memory, which is equivalent to **dat[44]**
16. The 0xB5 setting is 1-byte data read from **0x152D** of OTP memory, which is equivalent to **dat[45]**
17. The 0xE9 setting is 1-byte constant data of **0x01**.
18. The 0x30 setting is 1-byte constant data of **0x08**.

4. Input image to the EPD

This section describes how to send the image data into the COG driver which will update the display. The register index of image buffer is 0x10.

There is 2-bit data per pixel to define 4 colors. (e.g. the first byte represents the 1st ~ 4th pixels of the first line, the second byte represents the 5th ~ 8th pixels of the first line, …… and so on).

Data Byte	bit[7:6]	bit[5:4]	bit[3:2]	bit[1:0]
Pixel	pixel[n]	pixel[n+1]	P[n+2]	P[n+3]

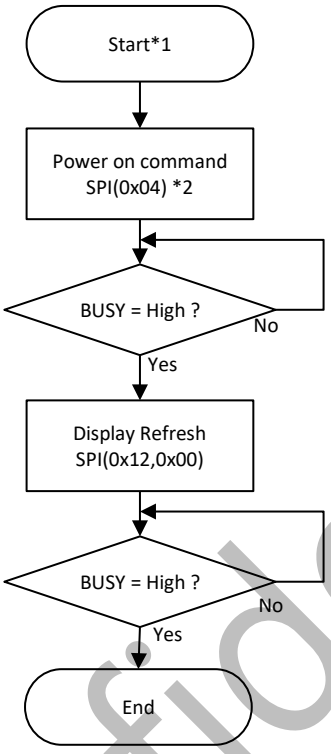



```
Image data input sequence:
Line001:(1,1)>(2,1)>…>(N,1)
Line002:(1,2)>(2,2)>…>(N,2)
                :
                :
                :
Line  M: ..... (N,M)

Frame data: 2 x N x M bits
          = (2 x N x M)/8 bytes

PD size     N     M    Total bytes
==================================
  1.54”    152   152      5,776
  2.13”    104   212      5,512
  2.66”    152   296     11,248
```

The color definition of image data is as blow table,

data	color
00	black
01	white
10	Yellow
11	Red

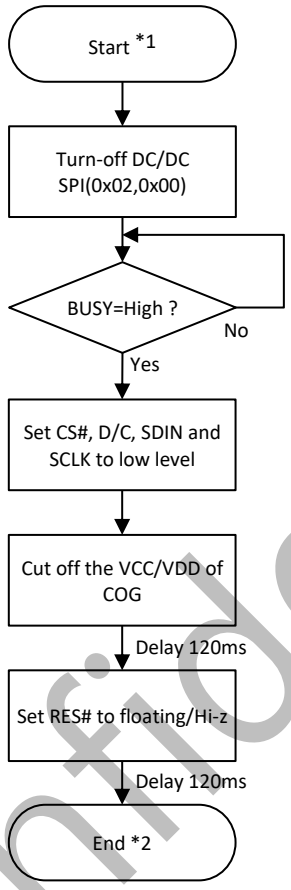
5. Send updating command



NOTE:

1. Start: Follow the end of the input image sequence
2. This register does not have data, just send the index

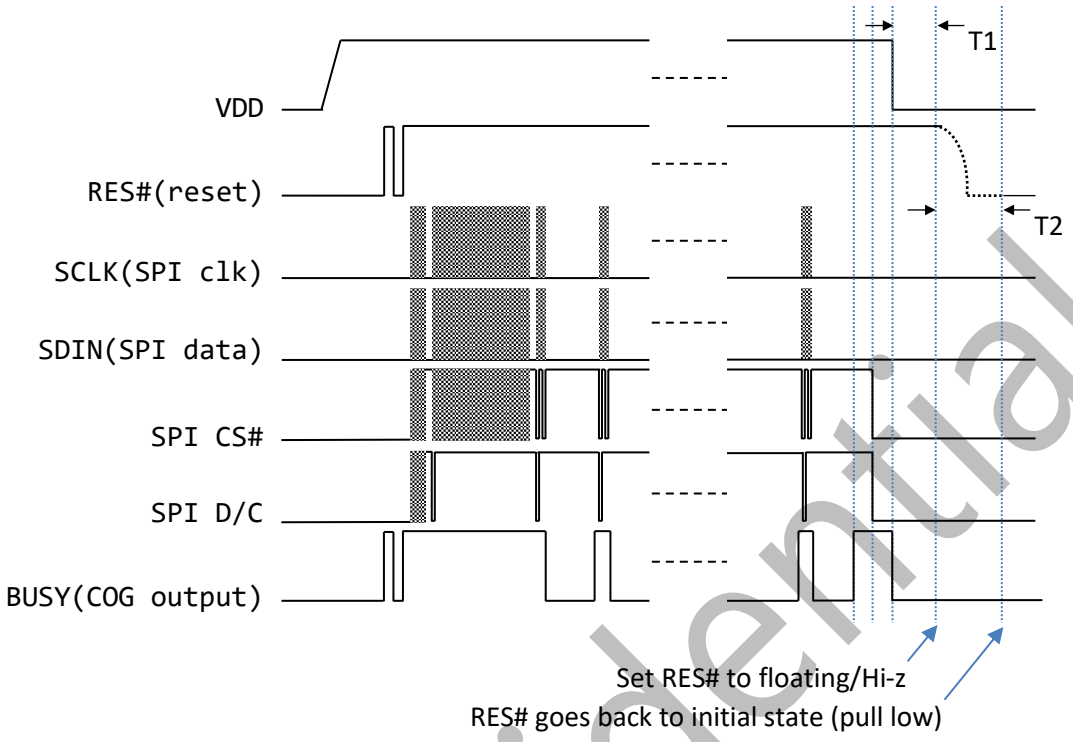
5. Turn-off DC/DC



NOTE:

1. Start: Follow the end of the send updating command
2. Finished all of procedure for update the EPD

This power-off sequence is exactly based on the application note provided by E-ink. The real timing diagram is like diagram on the next page. T1 and T2 must be more than 100ms at least.



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http://www.pervasivedisplays.com

Revision History

Version	Date	Page (New)	Section	Description
01	2023/5/22			First issue

Glossary of Acronyms

EPD	Electrophoretic Display (e-Paper Display)
EPD Panel	EPD
TCon	Timing Controller
FPL	Front Plane Laminate (e-Paper Film)
SPI	Serial Peripheral Interface
COG	Chip on Glass
PDI, PDi	Pervasive Displays Incorporated