Application Note

For

Pervasive Displays
BWRY 9.7” EPD

Description	**Elaborate how to refresh the Pervasive Displays 9.7” EPD**
Date	**2025/5/14**
Doc. No.	
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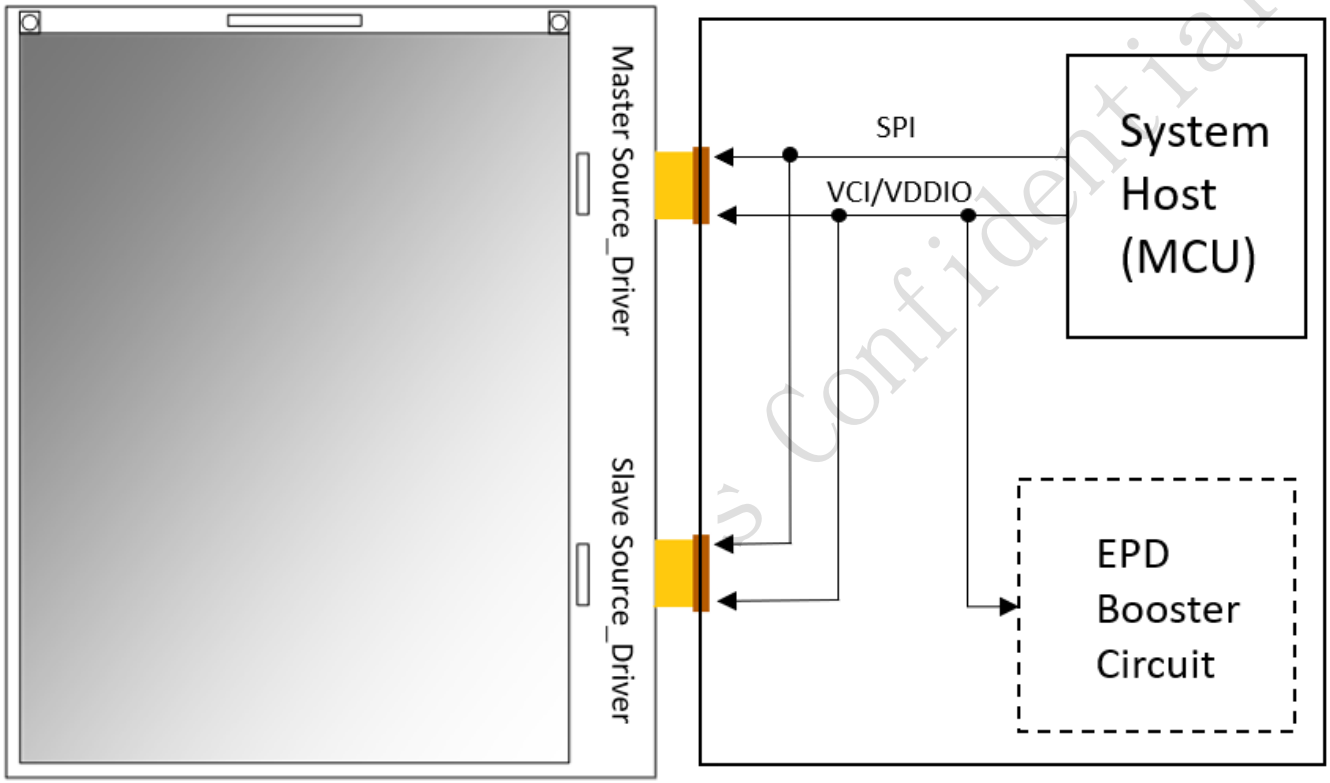
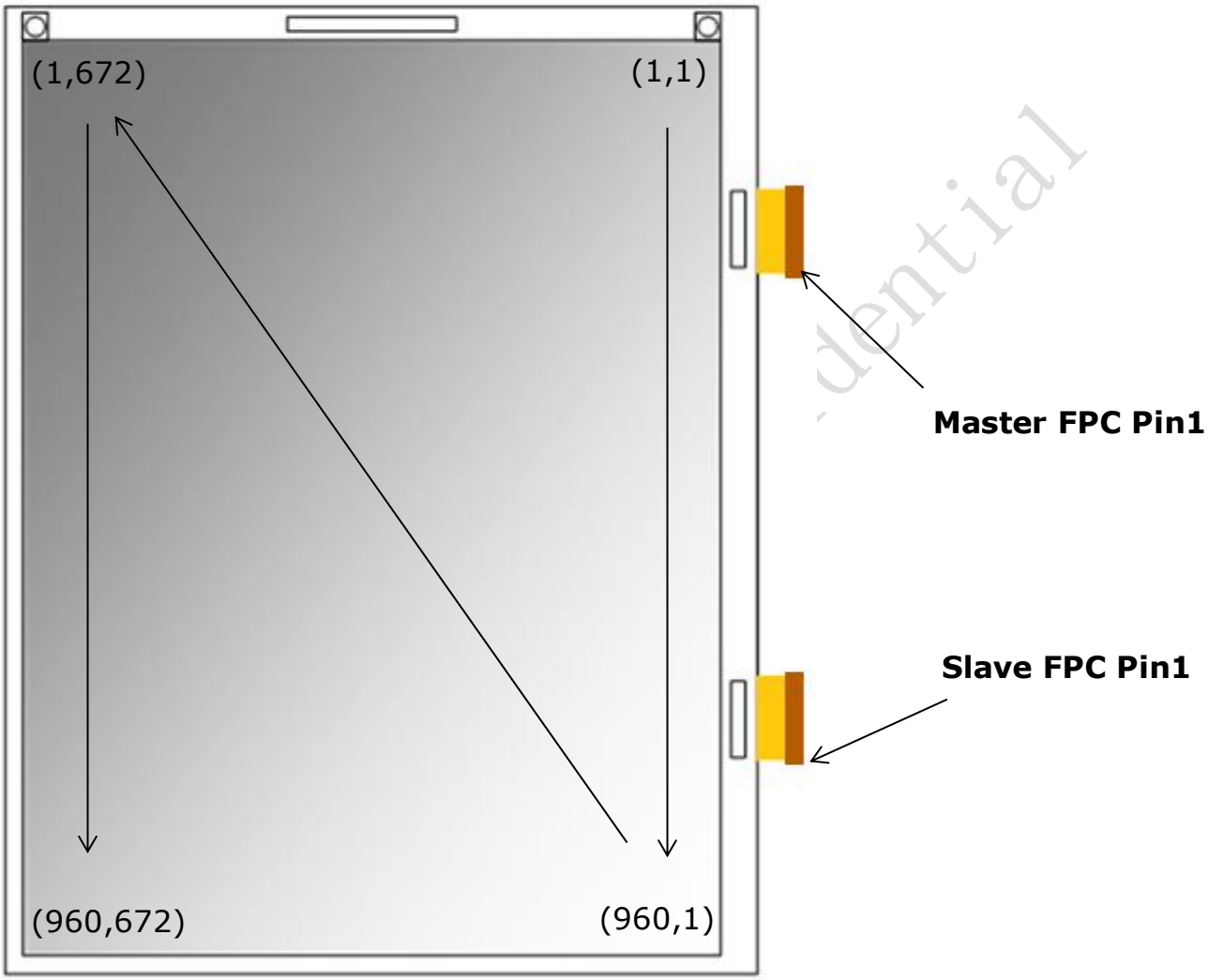
1. General Description

1.1 Overview

The document introduces how to drive the Pervasive Displays 9.7” BWRY EPD. The EPD has embedded the Tcon function. The driver's major control interface is SPI. The host sends the setting commands and the display image to the driver through the SPI bus.



1.2 Panel drawing



1.3 Interface

The 9.7" EPD was mounted two source drivers. They are Master and Slave role respectively and share the same SPI with separate CS.

The pin assignment of FPC are as follows, the pitch of FPC is 0.5mm.

1.3-1 Master FPC Pin Define

No.	Signal	Type	Connected to	Function
1	FSYNC	I/O	Slave FSYNC	Cascade line frame sync
2	NGDRV	O	Power MOSFET Driver control	This pin is the N-Channel MOSFET Gate Drive Control.
3	RESE	I	Booster Control Input	This pin is the Current Sense Input for the Control Loop.
4	INTERNAL_VPP	P	Master & Slave VPP Pin	MTP power (internal)
5	VDHR	C	Capacitor	This pin is the VDHR driving voltage. A stabilizing capacitor should be connected between VDHR and GND.
6	LNSYNC	I/O	Slave LNSYNC pin	Cascade line sync
7	CLK	I/O	Slave CLK pin	Cascade clock
8	BS	I	GND	This pin is setting panel interface.
9	M_BUSY	O	Device Busy Signal	This pin is Busy state output pin of the master chip. When Busy is an active, the operation of the chip should not be interrupted, and Command should not be sent.
10	RESETB	I	System Reset	This pin is reset signal input. Active Low.
11	DC	I	VDDIO or GND	This pin is Data/Command control.
12	M_CSB	I	VDDIO or GND	This pin is the Master chip select.
13	SCL	I	Data Bus	Serial communication clock input.
14	SDA	I	Data Bus	Serial communication data input/output.
15	VDDIO	P	Power Supply	Power for interface logic pins & I/O. It should be connected with VDDIO.
16	VDD	P	Power Supply	Power Supply for the chip.
17	VSS	P	GND	Ground
18	VDDL	C	Capacitor	Internal regulator output A capacitor should be connected between VDDL and GND.

No.	Signal	Type	Connected to	Function
19	VPP	P	INTERNAL_VPP& Slave VPP	MTP power
20	VDH	C	Capacitor	This pin is the Positive Source driving voltage. A stabilizing capacitor should be connected between VDH and GND.
21	VGH	C	Capacitor	This pin is the Positive Gate driving voltage A stabilizing capacitor should be connected between VGH and GND.
22	VDL	C	Capacitor	This pin is the Negative Source driving voltage. A stabilizing capacitor should be connected between VDL and GND.
23	VGL	C	Capacitor	This pin is the Negative Gate driving voltage. A stabilizing capacitor should be connected between VGL and GND.
24	VCOM	C	Capacitor	This pin is the VCOM driving voltage A stabilizing capacitor should be connected between VCOM and GND.

1.3-2 Slave FPC Pin Define

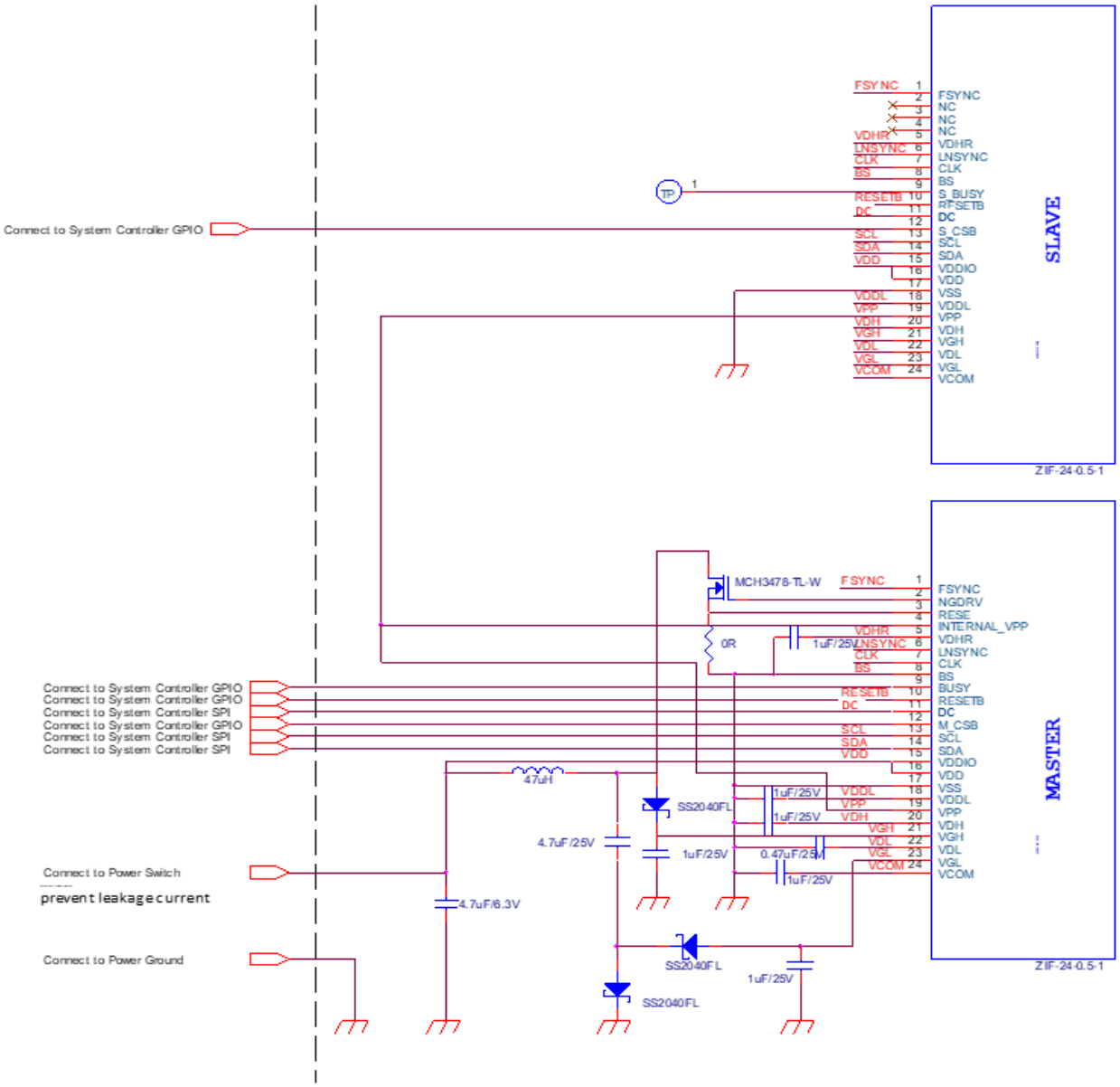
No.	Signal	Type	Connected to	Function
1	FSYNC	I/O	Master FSYNC pin	Cascade line frame sync
2	NC	-	-	Not connected
3	NC	-	-	Not connected
4	NC	-	-	Not connected
5	VDHR	C	Master VDHR Pin	This pin is the VDHR driving voltage. A stabilizing capacitor should be connected between VDHR and GND.
6	LNSYNC	I/O	Master LNSYNC pin	Cascade line sync
7	CLK	I/O	Master CLK pin	Cascade clock
8	BS	I	GND	This pin is setting panel interface.
9	S_BUSY	O	Device Busy Signal	This pin is Busy state output pin of the slave chip. When Busy is an active, the operation of the chip should not be interrupted, and Command should not be sent.
10	RESETB	I	System Reset	This pin is reset signal input. Active Low.

No.	Signal	Type	Connected to	Function
11	DC	I	VDDIO or GND	This pin is Data/Command control.
12	S_CSB	I	VDDIO or GND	This pin is the Slave chip select.
13	SCL	I	Data Bus	Serial communication clock input.
14	SDA	I	Data Bus	Serial communication data input/output.
15	VDDIO	P	Power Supply	Power for interface logic pins & I/O. It should be connected with VDDIO.
16	VDD	P	Power Supply	Power Supply for the chip.
17	VSS	P	GND	Ground
18	VDDL	C	Master VDDL Pin	Internal regulator output A capacitor should be connected between VDDL and GND.
19	VPP	P	INTERNAL_VPP	MTP power
20	VDH	C	Master VDH Pin	This pin is the Positive Source driving voltage. A stabilizing capacitor should be connected between VDH and GND.
21	VGH	C	Master VGH Pin	This pin is the Positive Gate driving voltage A stabilizing capacitor should be connected between VGH and GND.
22	VDL	C	Master VDL Pin	This pin is the Negative Source driving voltage. A stabilizing capacitor should be connected between VDL and GND.
23	VGL	C	Master VGL Pin	This pin is the Negative Gate driving voltage. A stabilizing capacitor should be connected between VGL and GND.
24	VCOM	C	Master VCOM Pin	This pin is the VCOM driving voltage A stabilizing capacitor should be connected between VCOM and GND.

Note:

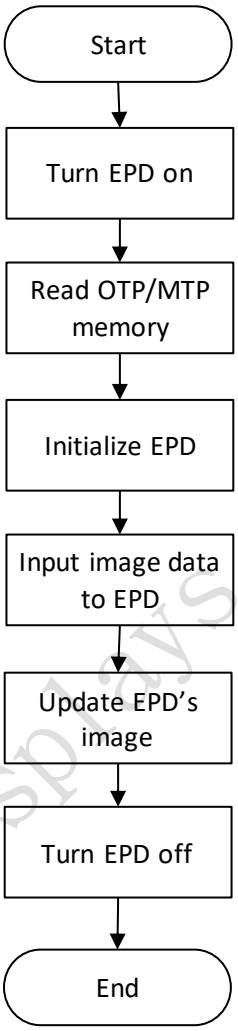
Type: I: Input
O: Output
C: Capacitor
P: Power

1.3-3 EPD Reference Circuit



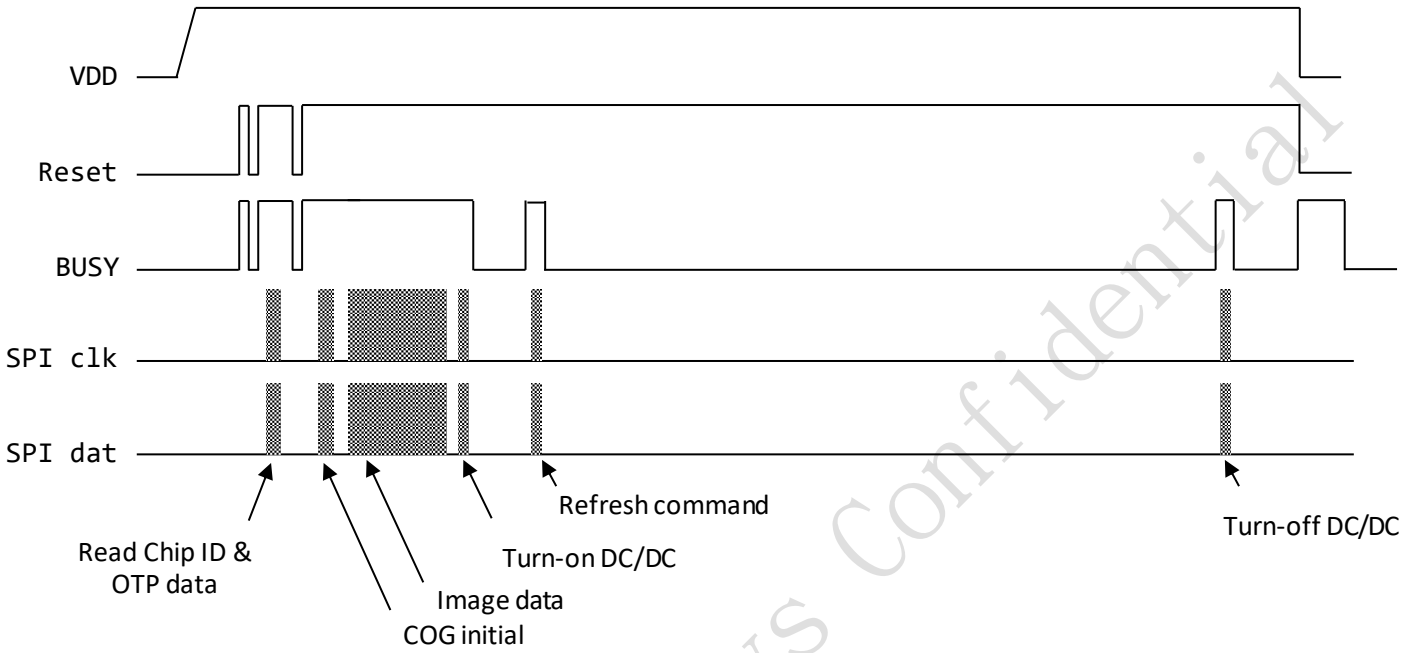
1.4 EPD Driving Flow Chart

The flowchart below provides an overview of the necessary actions to update the EPD. The steps below refer to the detailed descriptions in the respective sections.



1.5 Overall Waveform

The diagram below provides an overview of signal control during an EPD update cycle.



1.6 SPI Timing Format

SPI commands are used to communicate between the MCU and the COG Driver in EPD. The SPI format used differs from the standard. When setting up the SPI timing, Pervasive Displays recommends verifying both the SPI command format and SPI command timing in this section.

- SPI pins description:
  - SCLK : Serial communication clock.
  - SDIN : Serial communication data input/output

    When sending register index/data, the pin must be an output of the MCU.

    When reading data, the pin must be an input of the MCU.
  - D/C# : The pin is used to distinguish between the register index and data

    L : Register index. **H** : Data
  - M_CS# : Serial communication master chip select.
  - S_CS# : Serial communication slave chip select.

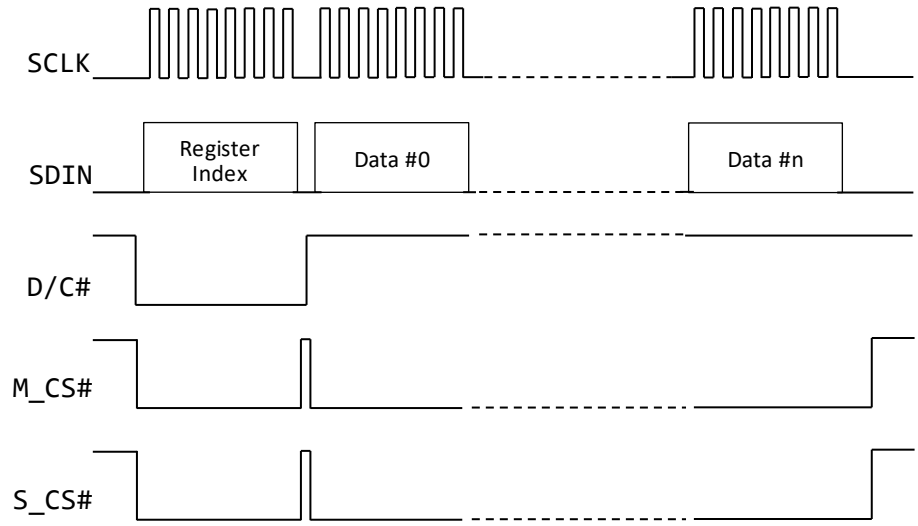
- Below is a description of the SPI Format:

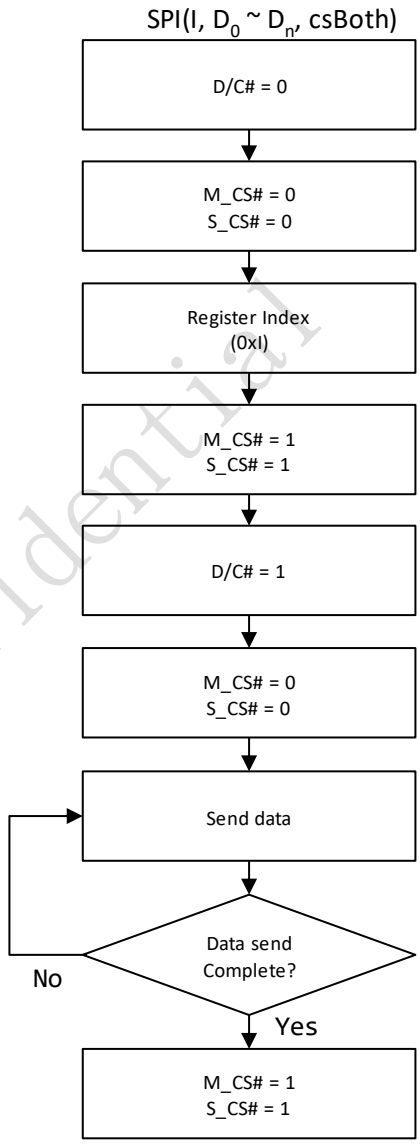
  SPI(0xI, 0xD_1, 0xD_2, …, 0xD_n, csDS)

  Where:

  I is the Register Index and the length is 1 byte
  $D_{1\sim n}$ is the Register Data. The Register Data length is varies.
  The csDS indicates this command is delivered to which driver or both.
  csMaster : only deliver to Master driver
  csSlave : only deliver to Slave driver
  csBoth : deliver to both Master and Slave

- SPI send command signals and flowchart:

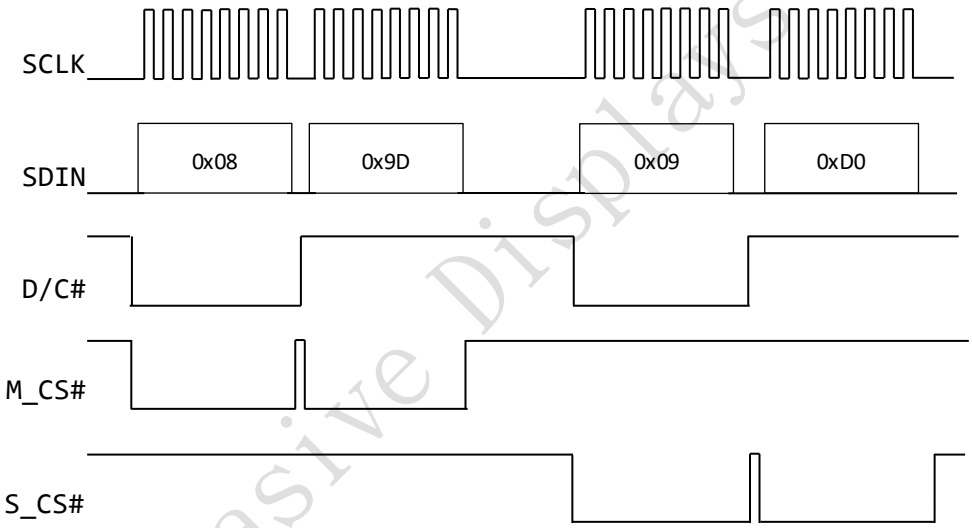




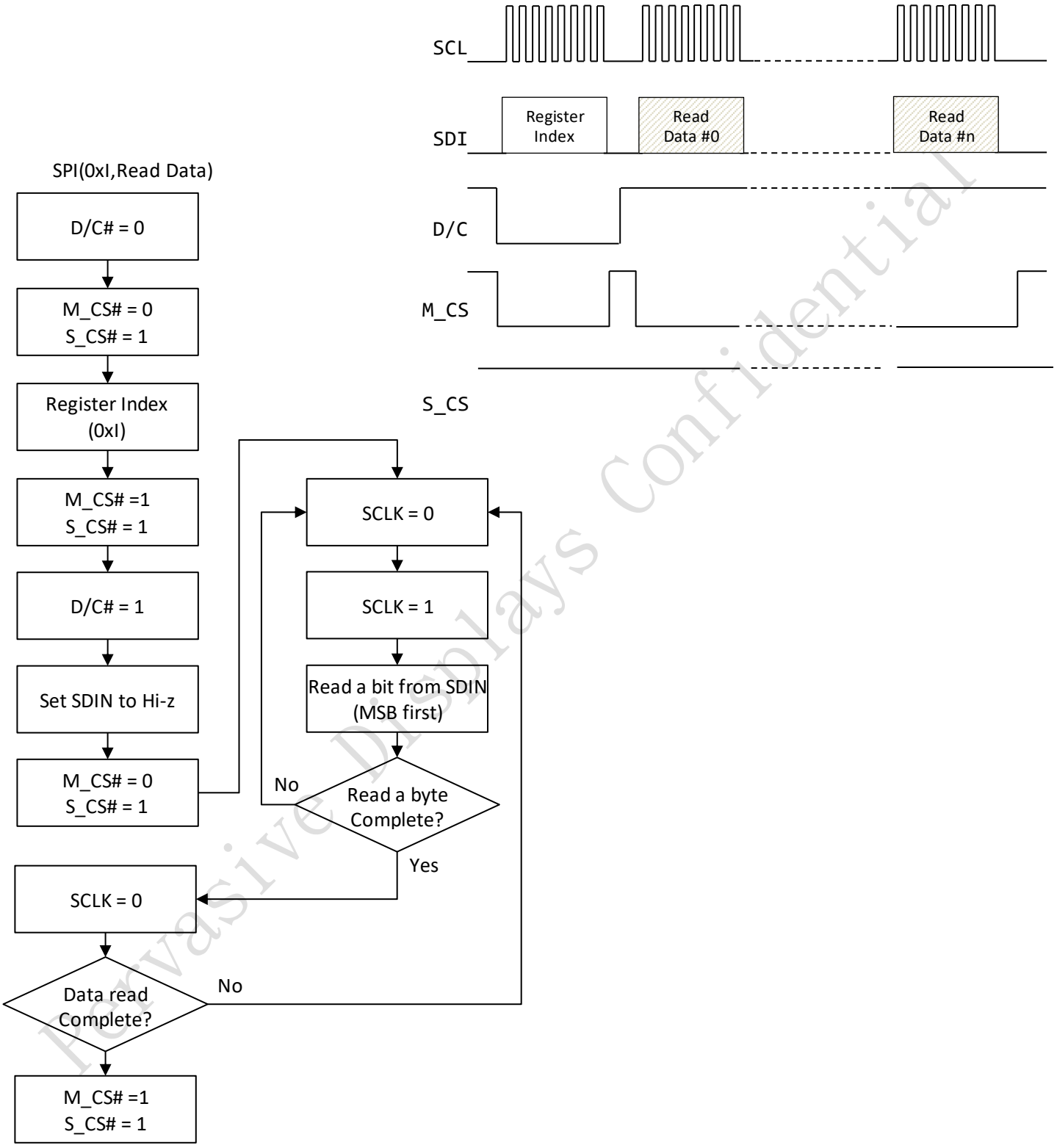
For example:

To send two SPI commands:

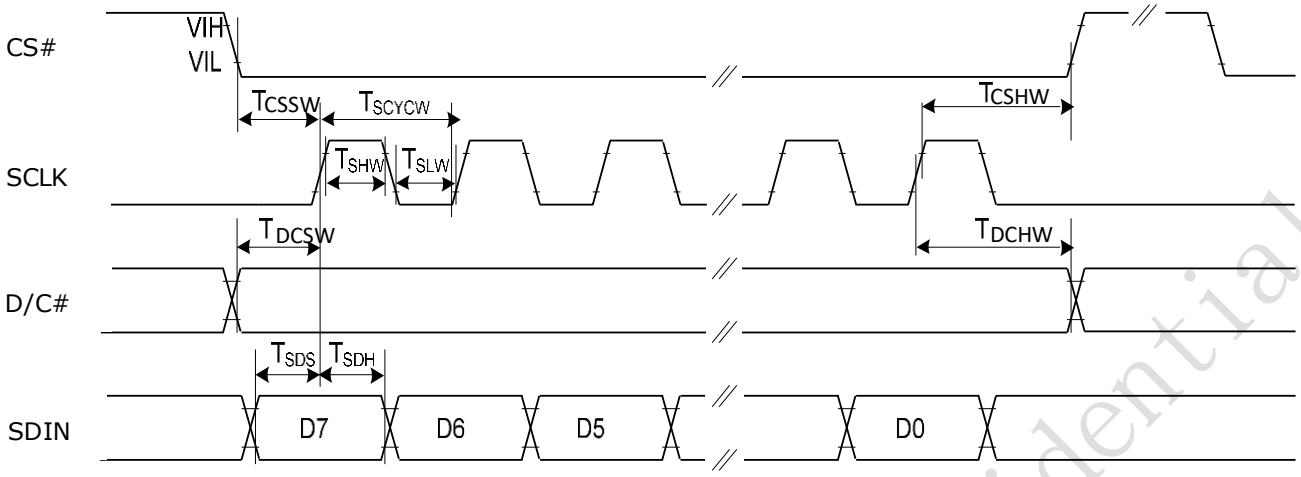
SPI(0x08,0x9D,csMaster) and SPI (0x09,0xD0,csSlave)



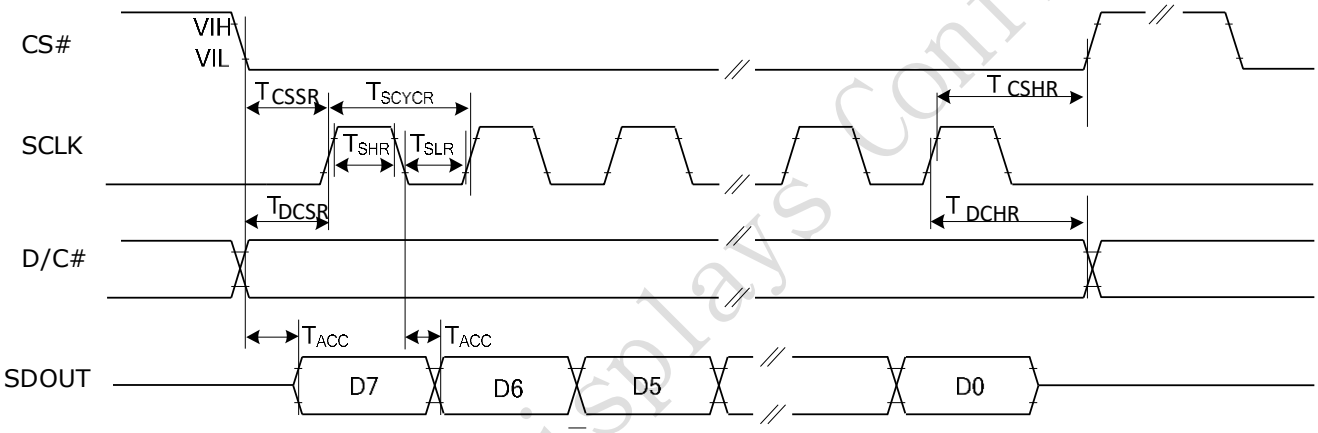
- SPI read command signals and flowchart:



- SPI command timing



Write mode



Read mode

AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Chip Select Setup Time(Write)	t_{CSSW}	60	-	-	ns	
Chip Select Hold Time(Write)	t_{CSHW}	65	-	-	ns	
Serial Clock Cycle (Write)	t_{SCYCW}	50	-	-	ns	
SCLK "H" Pulse Width (Write)	t_{SHW}	25	-	-	ns	
SCLK "L" Pulse Width (Write)	t_{SLW}	25	-	-	ns	
DC Setup Time(Write)	t_{DCSW}	5	-	-	ns	
DC Hold Time(Write)	t_{DCHW}	5	-	-	ns	
Data Setup Time	t_{SDS}	30	-	-	ns	
Data Hold Time	t_{SDH}	30	-	-	ns	
Chip Select Setup Time(Read)	t_{CSSR}	400	-	-	ns	
Chip Select Hold Time(Read)	t_{CSHR}	150	-	-	ns	
Serial Clock Cycle (Read)	t_{SCYCR}	600	-	-	ns	
SCLK "H" Pulse Width (Read)	t_{SHR}	150	-	-	ns	

SCLK "L" Pulse Width (Read)	t_{SLR}	400	-	-	ns
DC Setup Time(Read)	t_{DCSR}	90	-	-	ns
DC Hold Time(Read)	t_{DCHR}	90	-	-	ns
Access Time	t_{ACC}	-	-	200	ns

1.7 Read OTP memory mapping data

There are two sectors of memory in OTP that was programmed the User-defined data and the EPD initial data. This paragraph is going to describe the data format.

	USER-DATA BANK	ADDRESS	DATA	DESCRIPTION
OTP memory		0x0000 | 0x14FF	Pervasive Displays Reserves	
	BANK0	0x1500	check code	This check code indicates whether the BANK0 is valid. If so, it would be 0xA5
		0x1501 | 0x150F	Pervasive Displays Reserves	
		0x1510 | 0x1544	COG initial data	The data of this sector are the necessary IC initial data. These data need to be read out for IC initialization.
		0x1545 | 0x156F	Pervasive Displays Reserves	
	BANK 1	0x1570	check code	This check code indicates whether the BANK1 is valid. If so, it would be 0xA5.
		0x1571 | 0x157F	Pervasive Displays Reserves	
		0x1580 | 0x15B4	COG initial data	The data of this sector are the necessary IC initial data. These data need to be read out for IC initialization.
		0x15B5 | 0x15DF	Pervasive Displays Reserves	

According to the table, there are two memory banks to store two sets of user data. The "check code" is used to determine which bank is enabled. Based on the following procedures for reading the user data, the data from **0x1500** to **0x15DF** will be stored to the array **data[0] ~ data[223]**

Please note that all the command examples in this document assume that BANK0 is valid. Once the BANK1 is enabled, the element index of the data[n] would become data[n+0x70] to jump to the BANK1 area.

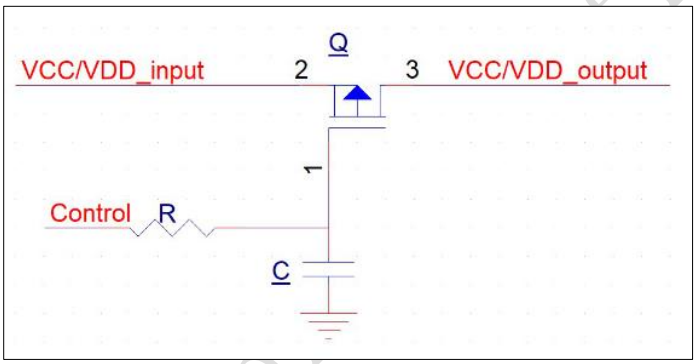
2. Turn on EPD

Turn on EPD processes

Step	Action / SPI instruction			
	Index	Data	Data size	Master/Slave
1	Initial state *1			
2	Turn on EPD's VDD/VCC *2			
3	COG reset *3			

Note:

1. Initial state the VCC/VDD, RES#, M_CS#, S_CS#, SDIN, SCLK, BS, D/C# = 0
2. In order to the inrush current will cause other issue. It is recommended to add soft-start when VCC/VDD is turned on. (as the circuit below)
3. Please refer to next page for details



- COG reset sequence

COG reset processes

Step	Action / SPI instruction			
	Index	Data	Data size	Master/Slave
1	RES# = 0			
2	Delay 20ms			
3	RES# = 1			
4	Delay 10ms			
5	RES# = 0			
6	Delay 20ms			
7	RES# = 1			
8	Delay 10ms			
9	Waiting for the BUSY signal to be high level			
10	Delay 10ms			

3. EPD initial

EPD initial processes [*1]

Step	Action / SPI instruction			
	Index	Data	Data size	Master/Slave
1	Read out the Chip ID from the 0x70 register to make sure it's right EPD [*2]			
2	0x90[*3]		0	Master
3	0xA2[*4]	0x00,0x15,0x00,0x00,0xE0	5	Master
4	Read out the user data from the 0x92 instruction [*5]			
5	COG Reset [*6]			
6	0xE6	Environment Temperature [*7]	1	Both
7	0xE0	0x02	1	Both
8	0xA5[*3]		0	Both
9	Waiting for the BUSY signal to be high level			
10	0x01	data[16] [*8]	1	Both
11	0x00	data[26,27,28]	3	Both
12	0x61	data[19,20,21,22]	4	Both
13	0x00	data[17,18,29]	3	Both
14	0x06	data[23,24,25]	3	Both
15	0x03	data[30,31,32]	3	Both
16	0xE7	data[33]	1	Both
17	0x65	data[34,35,36,37]	4	Both
18	0x30	data[38]	1	Both
19	0x50	data[39]	1	Both
20	0x60	data[40,41]	2	Both
21	0xE3	data[42]	1	Both
22	0xFF	0xA5	1	Both
23	0xEF	data[43,44,45,46,47,48,49,50]	8	Both
24	0xDC	data[59]	1	Both
25	0xDD	data[60]	1	Both
26	0xDE	data[61]	1	Both
27	0xE8	data[62]	1	Both
28	0xDA	data[63]	1	Both
29	0xFF	0xE3	1	Both
30	0xE9	0x01	1	Both

Note:

1. Start: Follow the end of the power on sequence
2. The 0x70 instruction can read out 2-byte data of the Chip ID that would be {0x0D,0x04}
3. This register does not have data, just send the index
4. The 0xA2 command was used to assign the start address for reading.
5. The first byte of read out is dummy byte. According to the OTP mapping table, the necessary data is from 0x01500 ~ 0x15DF, so there are 224 bytes data that need to be read out and store these data into the "**data**" array.
6. COG reset: please refer to the Ch.2

7. The data is temperature value and unit is degree of Celsius. The highest bit of the data represents positive/negative in temperature.

if it's positive, the data = (temperature value)

if it's negative, the data = (2's complement of temperature value)

example:

temperature value	data
25°C	0x19
5°C	0x05
-5°C	0xFB

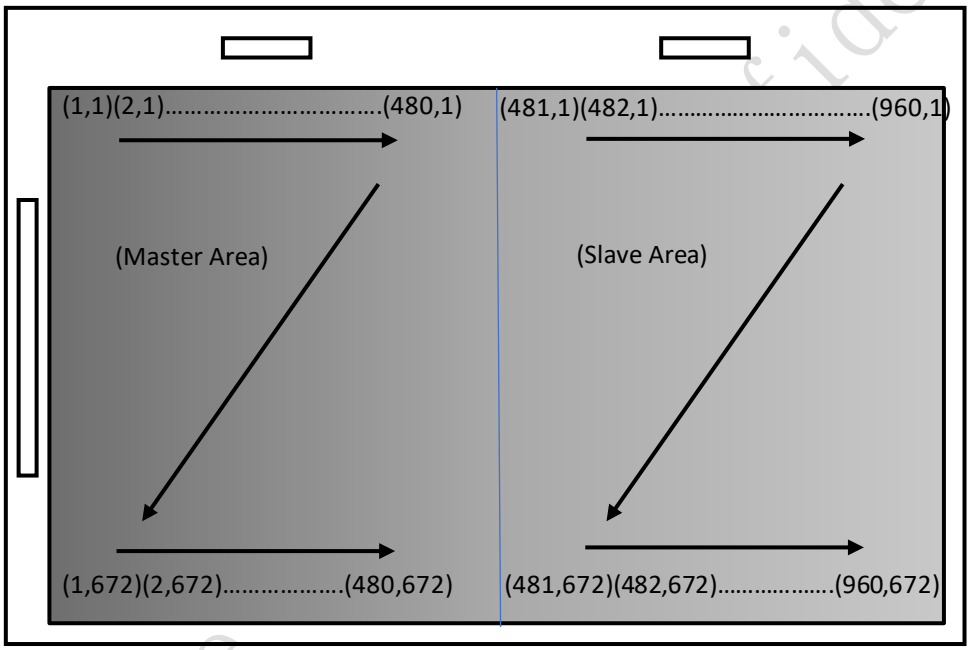
8. The command is with 1-byte data that would be read out from **0x1510** of OTP memory, which is equivalent to **data[16]**

4. Input image data to the EPD

This section describes how to send image data into COG which will be displayed on the display. The register index of the image buffer is 0x10.

There is 2-bit data per pixel to define 4 colors. (e.g. the first byte represents the 1st ~ 4th pixels of the first line, the second byte represents the 5th ~ 8th pixels of the first line, …… and so on).

Data Byte	bit[7:6]	bit[5:4]	bit[3:2]	bit[1:0]
Pixel	pixel[n]	pixel[n+1]	pixel[n+2]	pixel[n+3]



Master Image data input sequence:

Line001:(1,1)>(2,1)>…>(480,1)

Line002:(1,2)>(2,2)>…>(480,2)

:

:

:

Line672:.....(480,672)

Slave Image data input sequence:

Line001:(481,1)>(482,1)>…>(960,1)

Line002:(481,2)>(482,2)>…>(960,2)

:

:

:

Line672:.....(960,672)

Frame data : 2 x 960 x 672

= 1,290,240 bits

= 161,280 Bytes

The color definition of the image data is as follows,

data	color
00	black
01	white
10	Yellow
11	Red

5. EPD Update command

Update command *1

Step	Action / SPI instruction			
	Index	Data	Data size	Master/Slave
1	0x04*2		0	Both
2	Waiting for the BUSY signal to be high level			
3	0x12	0x00	1	Both
4	Waiting for the BUSY signal to be high level			

Note:

1. Start: Follow the end of the power on sequence
2. This register does not have data, just send the index

6. Turn off EPD

EPD off processes [*1]

Step	Action / SPI instruction			
	Index	Data	Data size	Master/Slave
1	0x02(POFF)	0x00	1	Both
2	Waiting for the BUSY signal to be high level			
3	0x00	0x07,0x2B,0x01	3	Both
4	delay 400 ms			
5	0xFF	0xA5	1	Both
6	0xEE	0xA0,0x1E	2	Both
7	delay 4ms			
8	0xEE	0x00,0x00	2	Both
9	delay 3ms			
10	0xFF	0xE3	1	Both
11	delay 6 sec.			
12	clear all IOs to low level[*2]			
13	delay 200ms			
14	Cut Vdd/Vcc off			
15	delay 120ms			

Note:

1. Follow the end of the EPD update command sequence
2. Set M_CS#, S_CS#, D/C, SDIN, SCLK, RESET to LOW level

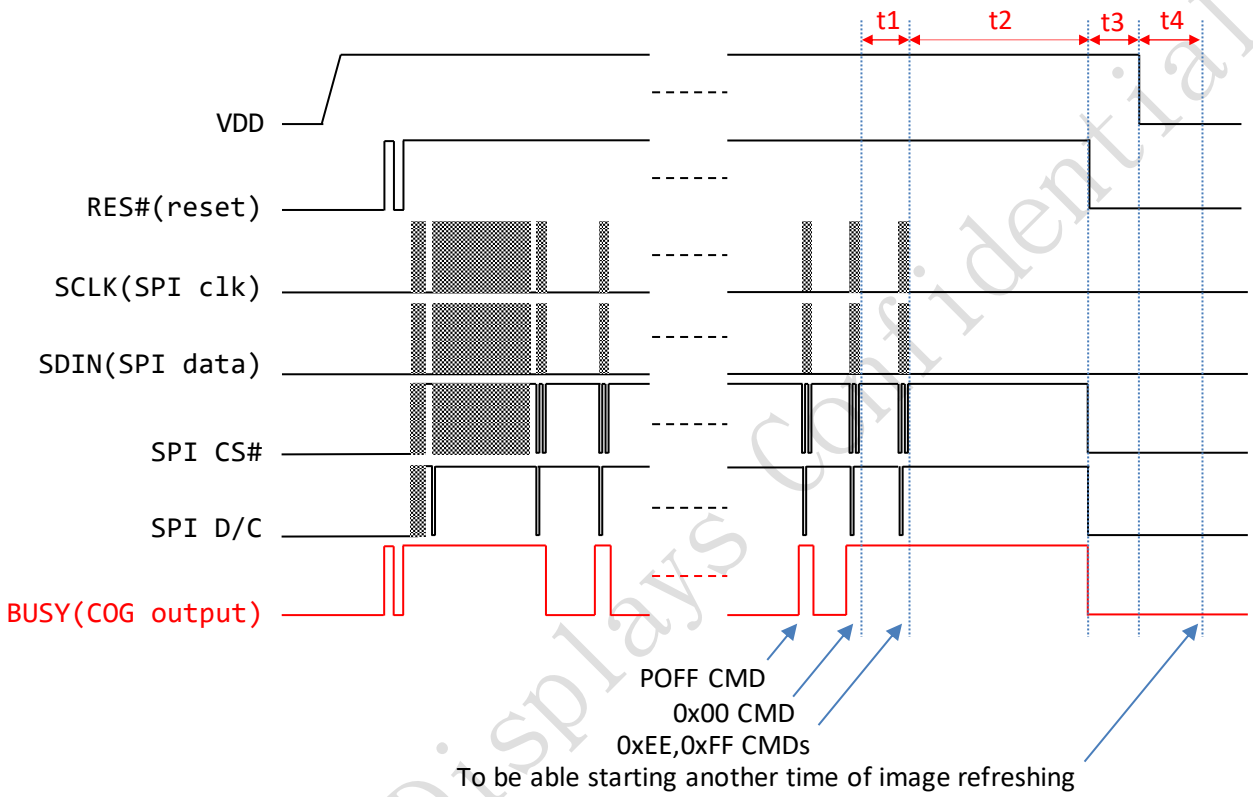
The power-off timing diagram is like the diagram below.

t1: more than 400ms.

t2: more than 6 second

t3: more than 200ms

t4: more than 120ms



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Revision History

Version	Date	Page (New)	Section	Description
v01	2025/5/14			Initial version

Glossary of Acronyms

EPD	Electrophoretic Display (e-Paper Display)
EPD Panel	EPD
TCon	Timing Controller
FPL	Front Plane Laminate (e-Paper Film)
SPI	Serial Peripheral Interface
COG	Chip on Glass
PDI, PDi	Pervasive Displays Incorporated